2-6 GHZ GALLIUM NITRIDE HEMT MMIC AMPLIFIER DESIGN

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ABSTRACT

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Wideband RF power amplifiers are critical components in many electronic systems such as communication systems, radars and electronic warfare systems. Chip size, output power, efficiency and reliability are key points of the performance of those electronic systems. Recently, Gallium Nitride (GaN) high electron mobility transistors (HEMTs) are widely used to satisfy system requirements. GaN HEMT process provides high output power, high efficiency and reliability performance at microwave frequencies due to its wide band gap properties [1]. In this thesis, 2-6 GHz GaN MMIC driver amplifier is designed with 5 W output power and 40% power added efficiency (PAE). In this type of broadband amplifiers, undesirable performance drops can be observed because of the harmonics effect. To achieve target RF performances in the first production, matchings are modified by considering harmonics. Advanced Design System (ADS) software program is used during design. Fabrication and measurement steps are also performed. In this work, remarkable RF performances are achieved compared with similar examples.

Keywords: GaN HEMT, Driver Amplifier, MMIC, Output Power, PAE

ÖZ

2-6 GHZ GALLIUM NITRIDE HEMT MMIC YÜKSELTEÇ TASARIMI

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Geniş bant radyo frekansı güç yükselteçleri iletişim, radar ve elektronik harp gibi birçok sistemin kritik parçalarındandır. Çip boyutu, çıkış gücü, verimlilik ve güvenilirlilik bu elektronik sistemlerin performansının anahtar noktalarıdır. Sistem gereksinimlerini sağlamak için son zamanlarda Galyum Nitrür (GaN) HEMT teknolojisi sıklıkla kullanılmaktadır. GaN HEMT prosesi geniş bant aralığı özelliği sayesinde mikrodalga frekanslarında yüksek çıkış gücü, yüksek verimlilik ve güvenilirlilik performansı sağlamaktadır [1]. Bu tezde, 5 W çıkış güçlü, 40% yük ekli verimliliğine sahip 2-6 GHz GaN MMIC sürücü güç yükselteci tasarlanmıştır. Geniş bantlı yükselteçlerde, harmonik etkilerden kaynaklı olarak, istenmeyen performans düşüşleri gözlemlenebilir. İlk üretimde hedeflenen RF performanslarını elde edebilmek için, harmonikler dikkate alınarak, eşlemeler değiştirildi. Tasarım sırasında Advanced Design System (ADS) programı kullanılmıştır. Fabrikasyon ve ölçüm aşamaları da gerçekleştirilmiştir. Bu çalışmada, benzer örneklere kıyasla dikkate değer RF performansları elde edilmiştir.

Anahtar Kelimeler: GaN HEMT, Sürücü Güç Yükselteci, MMIC, Çıkış Gücü, Güç Çekim Verimliliği

To my Family

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INTRODUCTION

1.1 RF MMIC Amplifier

In most RF and microwave systems such as radar and radio transmitter/receiver modules, high output powers are essential to satisfy system requirements. For this purpose, RF amplifiers are designed and manufactured to amplify signals [2]. They are generally used at the end stage of the systems to transmit high output power. Basically, RF amplifiers convert supplied DC input power to high level RF output signal. In early times of RF technology, vacuum tube amplifiers, such as klystrons and traveling-wave tube amplifier (TWTA), have been commonly used to satisfy high RF requirements of RF/microwave systems. Vacuum tube amplifiers control the electrons movement and absorb the energy from those electrons to achieve signal amplification. Those tube amplifiers, however, have huge dimensions and reliability issues. In recent microwave applications, solid state amplifiers are used commonly rather than bulky tube amplifiers since they are low cost, much smaller, more efficient, more reliable and easy to integrate in systems. Another significant advantage of solid state amplifiers is they can be manufactured at high number easier than vacuum tubes. As a disadvantage, however, solid state amplifiers cannot provide huge output power, in gigawatts, as vacuum tubes. For some applications, vacuum tubes are still used if extreme RF output power levels are needed.

Recently, GaN on Silicon Carbide (SiC) semiconductor amplifiers are popular in microwave systems due to important advantages, such as high breakdown voltage, high current density, high operation supply voltage and high output power [3]. All active and passive circuit elements, like transistor, inductor and capacitors, are manufactured on a Gan on SiC semiconductor substrate in MMIC chips. MMIC dies

are fabricated in wafers which include many MMIC circuits. This advantage reduces the cost of a RF MMIC amplifier.

1.2 GaN HEMT Technology

The significant progress for solid state devices was started with the invention of transistors. Then, gallium arsenide field effect transistor (FET) and silicon bipolar transistors were developed in the late 1960s [4]. This FET invention is another milestone for RF and microwave area, especially for solid state devices. After FETs development, new solid state structures were developed such as HEMT, HFET and HBT on new semiconductors, like InP, SiC, GaAs and GaN [5]. These technologies help to achieve amplification at higher frequencies up to 100 GHz. HEMTs especially differ from other structure since they consist of several layers of semiconductor material. GaN technology is quite new and promising semiconductor technology. A cross section of a GaN HEMT structure is shown at Figure 1.1 [6]. A two dimensional electron gas (2DEG) region occurs between AlGaN/GaN barrier and GaN channel by different doping level. This 2DEG region increases electron mobility at high frequencies.

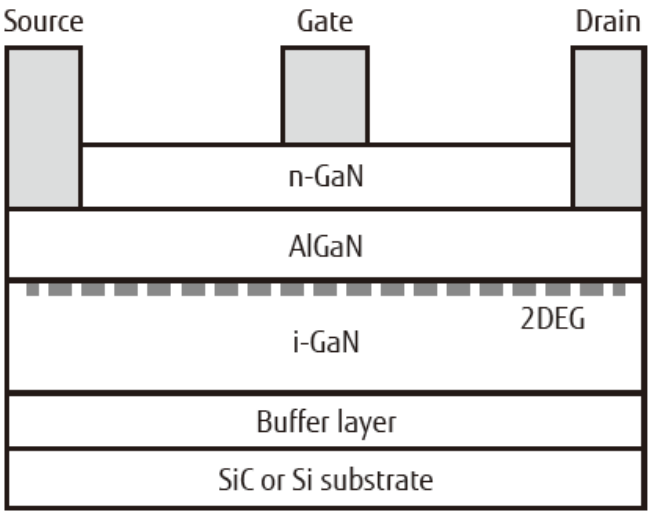


Figure 1.1. Cross Section of AlGaN/GaN HEMT Structure [6]

This GaN on SiC HEMT technology offers high output power and high efficiency levels because of GaN large bandgap properties such as high breakdown voltage, high current density, high operating voltage [7]. Table 1 shows the material properties of commonly used semiconductors [8]. It can be seen that GaN HEMT structure has higher bandgap which results as higher critical field, higher breakdown voltage. Therefore, higher supply voltage operation is possible for GaN HEMTs, such as 100 V drain supply. Another example for technology comparison is shown at Figure 1.2 [9]. It seems that higher power can be achieved at microwave frequency with GaN on SiC process. Also, it has high thermal conductivity which is critical for reliability issue at high power operation.

Table 1.1. Material Comparison of wide bandgap materials [8]

Material	Bandgap (eV)	Mobility, μ (cm^2/V.s)	Permittivity	Vsat (cm/s)	Critical Field (V/cm)
Si	1.1	1400	11.8	1×10^7	3×10^5
GaAs	1.42	8500	12.8	2×10^7	4×10^5
4H-SiC	3.23	260	9.7	2×10^7	2.9×10^6
GaN (Bulk)	3.4	900	9	2.5×10^7	3.3×10^6
GaN (HEMT)	3.4	1800	9	2.5×10^7	3.3×10^6

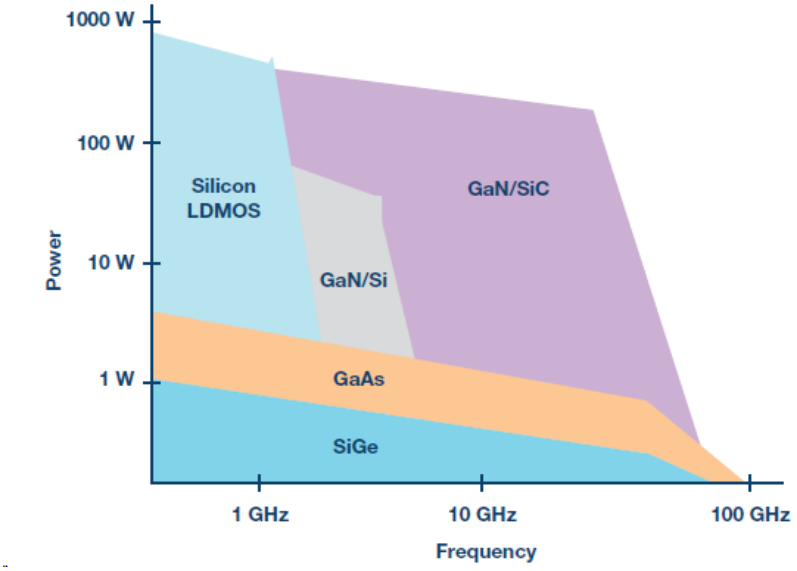


Figure 1.2. A process technology comparison at microwave frequency [9]

Reducing the system size and weight of the RF components is critical requirement for today's RF systems. Because of the higher power densities, increased efficiency and higher thermal conductivity properties of GaN on SiC process with respect to GaAs and travelling-wave tubes (TWT), smaller size RF board systems can be achieved [10]. Higher power density provides less combining of dies to achieve same output power target. This less combining results not only reduced board size, but also lower system losses and lower power requirements. Figure 1.3 shows an example to understand advantage of GaN on SiC process over GaAs [10]. This GaN devices also have higher output impedance levels. Due to this higher output impedance level, matching structures for transistors can be designed with less components and this provides smaller size matching structures [11]. In this thesis, one goal is to obtain the target power at smaller size. Main disadvantage of GaN semiconductor process is its higher cost since it's quite new process.

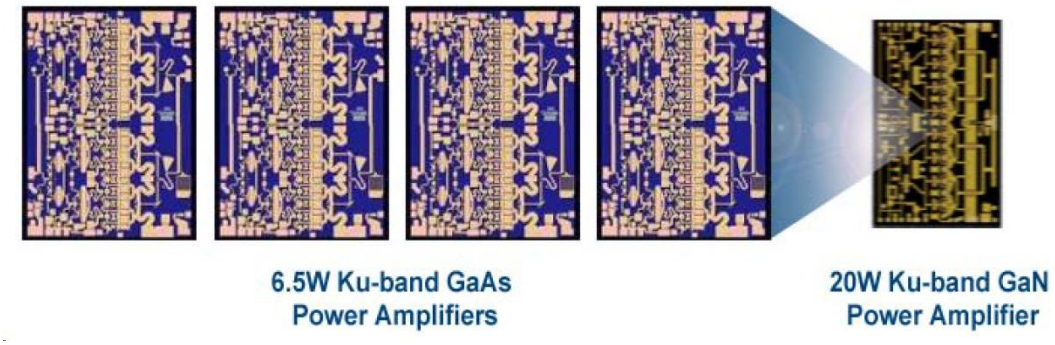


Figure 1.3. An example for GaN amplifier advantage on GaAs amplifiers [10]

1.3 Motivation of the Work

First production success is critical for GaN process amplifiers because of its higher cost and longer manufacturing time. In broadband amplifiers, second and third harmonics of fundamental operation frequencies may decrease the RF performance since they are in the operation band. For instance, harmonics of 2 GHz and 3 GHz are in operation band for this 2-6 GHz GaN amplifier. Effect of these harmonics should be examined to prevent undesirable RF performance decrement around specific frequency region. In this work, two different versions of the amplifier are presented to satisfy the first production success. In one version, impedances in only fundamental frequencies are taken into account while harmonics also are analyzed in other one. Matchings are improved to obtain higher RF performances in all operation band with respect to other GaN die examples.

In MMIC amplifier designs, large signal models of transistors are not accurate to observe exact power and efficiency performances since they are based on extrapolations rather than measurements. To perform a successful design, selected transistors can be modelled by large signal measurements. However, this is quite expensive and difficult process which needs lots of time and trials. Therefore, small signal measurements of transistors are performed to obtain S-Parameters. Selected transistor cells are manufactured before the amplifier design for the small signal measurements. Obtained S-Parameter data of transistors are used during the

amplifier design to obtain compatible simulation results with measurements. This procedure increases the chance of first production success.

1.4 Thesis Outline

In this thesis, design and analysis of two different versions of 2-6 GHz 5 W, 2 stages monolithic microwave integrated circuit (MMIC) amplifier are presented. All design procedure and measurements are included in the thesis work. Main targets are 5 W output power and 40% power added efficiency (PAE) and 30 dB small signal gain. To satisfy all these requirements, commercially avaliable 0.25 μm GaN on SiC high electron mobility transistor process is used.

Fundamentals of RF MMIC power amplifiers, performance parameters, design techniques and analysis are described in Chapter 2. Then, thesis continues with design procedure of the amplifier and simulation results in Chapter 3. All measurements are presented in Chapter 4. Finally, the thesis is concluded and future plans are explained in Chapter 5.

CHAPTER 2

FUNDAMENTALS OF RF MMIC AMPLIFIERS

Each RF power amplifier provides its specific performance with respect to its design details. These specific performance requirements are determined separately for each system. Main performance terms of an RF amplifier are output power, stability, efficiency, gain, bandwidth, input return loss, output return loss and linearity. To achieve target performances, different types of design techniques have been used. In this chapter, power amplifier fundamentals are described by concerning these important performance requirements and design details.

2.1. Stability

Stability can be considered as the most critical parameter of an RF amplifier. If the circuit is not stable, it cannot provide any other specifications. The circuit cannot be defined as an amplifier. Even and odd mode stability analysis are the main types to be analyzed. Stability can be investigated by two different mathematical methods. Rollet's and Nyquist stability analysis are famous methods to determine circuit stability performance. Rollet's method uses two factors which are K and μ factors. According to Rollet's stability analysis (K-Δ test), a two port network is defined as unconditionally stable for all passive load and source terminations, if two factors satisfy following conditions simultaneously [2].

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{21}S_{12}|} > 1 \quad (2.1)$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (2.2)$$

Nyquist stability analysis is another method discussed in this section. In Nyquist stability analysis, each stage of an amplifier is analyzed from input and output sides of transistors. Reflection coefficients from input and output sides of each individual transistor are multiplied as given by equation (2.3).

$$G = -(\Gamma_{in} \times \Gamma_{out}) \tag{2.3}$$

The magnitude of this product should be smaller than 1. Instability can be observed especially if the product passes from '-1+0j' point in counter-clockwise direction [12]. An example to show how Nyquist stability analysis can be performed is shown at Figure 2.1 [12]. Transistors are driven from port I, then reflection coefficients from both input and output sides are multiplied. Nyquist analysis is used if there are multiple transistors at one stage.

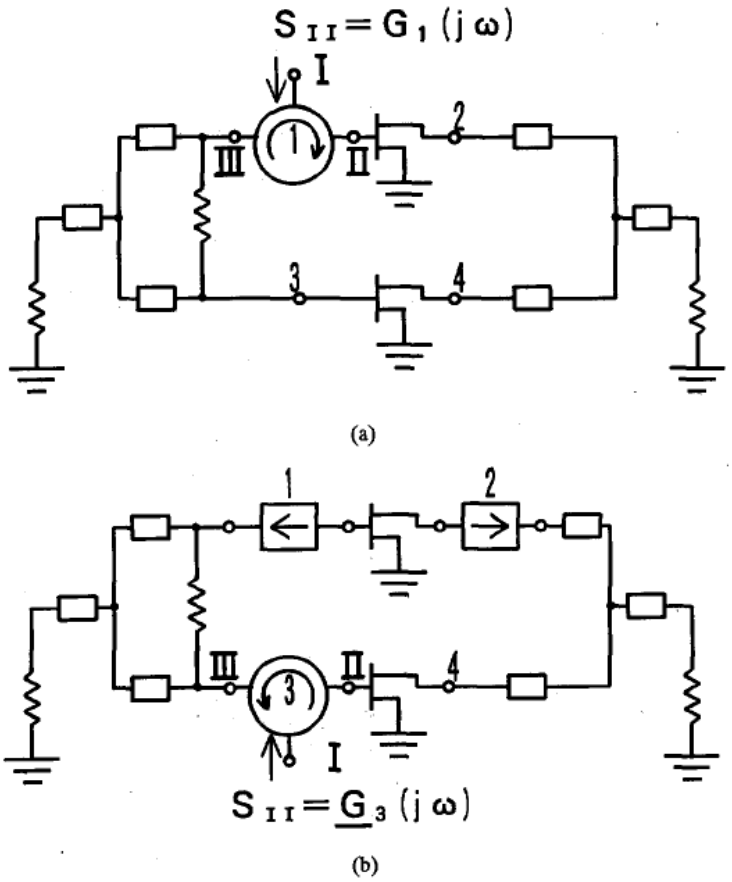


Figure 2.1. An example circuit for calculating reflection coefficients [12]

2.2. Efficiency

Efficiency is another critical parameter of an RF amplifier. An RF amplifier basically converts DC input power to RF output power and efficiency measures this conversion. Efficiency directly affects the thermal performance of the amplifier. Higher efficiency means higher thermal performance and this improves performance of the circuit. Also, efficiency can affect reliability of the circuit as well. Higher efficiency can increase lifetime of the circuit.

Three different versions of efficiency are defined for an amplifier. One of them is drain efficiency. It is directly obtained by RF output power and DC input power. It's the ration of output obtained RF power to consumed DC power.

$$\text{Drain Efficiency} = \frac{P_{out,RF}}{P_{DC}} \tag{2.4}$$

The other efficiency criteria is the power added efficiency (PAE) which is used as state of the art for RF MMIC amplifiers. This takes RF input power into account. If gain of the amplifier is high, drain efficiency is close to PAE.

$$\text{PAE} = \frac{P_{out,RF} - P_{in,RF}}{P_{DC}} \tag{2.5}$$

Overall efficiency is another efficiency definition which considers all input power.

$$\text{Overall Efficiency} = \frac{P_{out,RF}}{P_{DC} + P_{in,RF}} \tag{2.6}$$

2.3. Classes of Amplifiers

For an amplifier design, one of the important steps is to select bias condition determined by gate and drain DC voltages of the transistors. These DC voltages are called as quiescent point or Q-point, which effects linearity, gain, output power and efficiency performance of an amplifier. RF power amplifiers are generally classified as class A, B, AB, C, D, E and F with respect to their Q-point and matching types. Transconductance amplifiers are mainly operated as class A, B, AB, C while other classes, class D, E and F, are used for switching-mode amplifiers. Efficiency and linearity are main trade-off performances for these classes. Transconductance amplifiers have better linearity, but they sacrifice from efficiency and vice versa for switching amplifiers [13].

Transistors operate as switches in class D and class E amplifiers. In 'ON' state transistor impedance is very low with respect to the load impedance. Therefore, power dissipation is ideally zero, if transistor on state resistance is negligible. In 'OFF' state transistor impedance is very high, so that there is no current flow. In other words, there is a 180º phase difference between voltage and current waveforms at the output. These result as 100% drain efficiency in ideal case for class D and class E. However, because of the non-ideality of transistors, drain efficiency is lower than 100%, but still much higher than other classes.

High efficiency level can be obtained in class F amplifiers by a different impedance matching method. Harmonic impedance matchings are performed with resonators in output matching circuit. Since these harmonic matchings can be applied to only finite number of harmonic levels, 100% efficiency, which is achievable in theory, cannot be obtained. Despite all this efficiency advantage, octave bandwidth operation is not achievable in class F amplifiers.

The input sinusoidal signal is conducted continuously for a full cycle (360º) of the signal in class A amplifier. They are the most linear, but the least efficient amplifiers compared to other classes. Maximum achievable drain efficiency of a class A amplifier is 50% for no saturation case [13]. To have better efficiency, an amplifier

can be operated at class B. The conduction is only half-cycle (180º) of input sinusoidal signal for class B. To satisfy this half conduction, meaning higher efficiency, an amplifier is biased at the pinch-off voltage of the active device. Theoretically, maximum achievable drain efficiency of a class B amplifier is 78.5% [13]. However, class B amplifiers have lower linearity than class A amplifiers. Between class A and B, there exists class AB operation. The conduction of the input signal is higher than a half cycle for this middle class. A class AB amplifier has higher efficiency than class A and better linearity than class B. These three classes bias points are shown in Figure 2.2 as a graph of drain source current vs. drain source voltage [13].

Target power added efficiency of this thesis study is 40% which is quite high with at least 5 W output power. To satisfy these requirements, class AB is chosen because of its optimum performances for transconductance amplifiers. This class of biasing provides higher efficiency with improved linearity as requested in this thesis work.

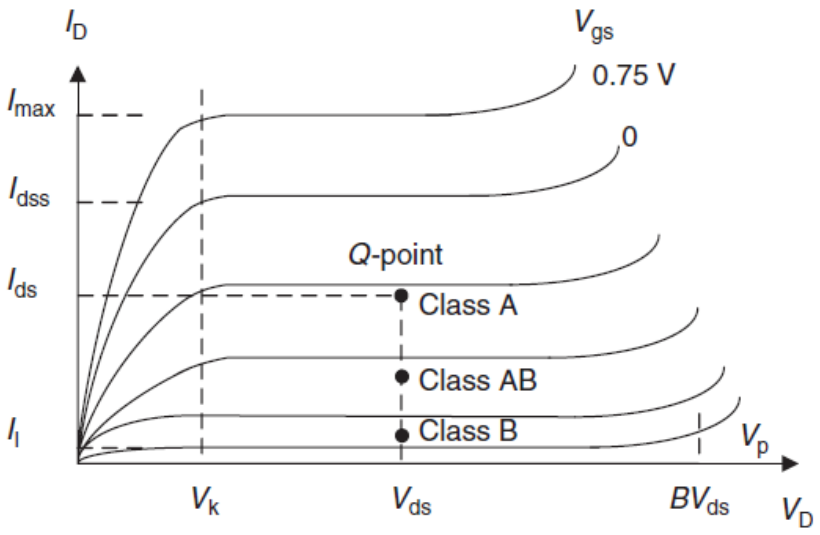


Figure 2.2. Biasing graph for different classes [13]

2.4. Load Pull Measurement and Simulation

Transistor performance is significantly affected by impedances seen from gate and drain. Especially transistor output power, PAE and gain is determined by impedances. Each performance needs its separate optimum impedances. Meaning, for maximum output power transistor should see an optimum power load and for maximum PAE transistor should see another optimum efficiency load. These optimum loads are satisfied by matching circuits which include high and low pass filters, capacitors, inductors and resistors. Before starting matching, optimum impedances should be found. These optimum load points can be found by Load-Pull. Both simulation and measurement can be applied for Load-Pull. Large signal transistor model is used for simulation at the software and large signal models may not be accurate since nonlinear behavior modelling is quite hard. To achieve success at first iteration, best way is to use Load-Pull measurement result. Each load impedance is swept at Smith Chart while output power, efficiency and gain results are recorded for each load point at Smith Chart. Then, results are showed as circles at Smith Chart which show power and efficiency levels with respect to load points. Figure 2.3 shows an example for Load-Pull result. This Load-Pull measurement can be done on-wafer by probes, so that optimum load points can be determined exactly from transistor sides without taking account of any other component. Automated tuner which moves impedances to every point at Smith Chart, network analyzer (PNA-X), on-wafer probes, a computer, a complex software, on-wafer station, bias tees and driver amplifier are used for a Load-Pull measurement. In this thesis, load-pull measurement is used for output stage transistor (much critical) and load-pull simulation is used for driver stage transistor.

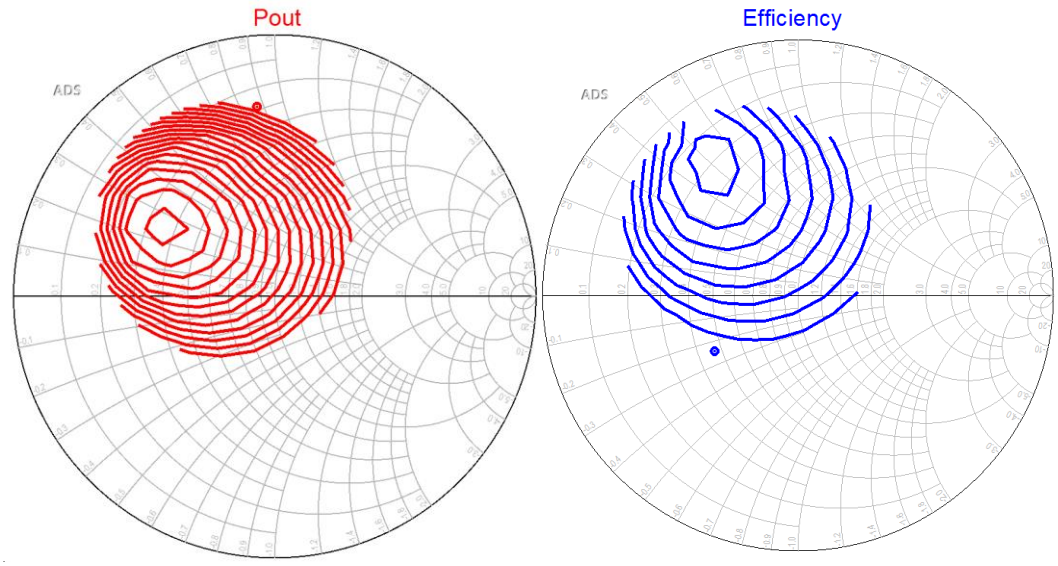


Figure 2.3. 8×200 μm Transistor Load-Pull Measurement Result Example

2.5. Matching Types

Impedance seen from transistors' output and input should be matched to target points which are determined by load-pull and source-pull measurements. To satisfy these matching and obtain target performances, there are different matching topologies. In this part of the thesis, three types of the matching topologies are discussed. These are harmonic reaction amplifiers, reactive matching amplifiers and distributed amplifiers.

First matching topology discussed in this part of the thesis is harmonic reaction matching. Different special circuits are applied to have high efficiency level in harmonic reaction amplifiers. Harmonics of the fundamental operation frequencies are considered at both source and load side of the transistors in this topology. Also, special biasing methods are applied to obtain switching from drain current and voltage waveforms. Up to 70-80% drain efficiency values can be realized due to this special matching and biasing techniques [14]. These efficiency levels are the highest achievable values between three topologies. However, bandwidth of the operation frequency is narrowband which means that relation between upper and lower operation frequencies is limited by 1.1:1 to 1.2:1 [15].

The second matching topology discussed in this section is the distributed matching. Amplifiers with distributed matchings are also called traveling-wave amplifiers. Distributed matching topology is used commonly in GaN and GaAs MMIC amplifiers which need ultra wideband operation. Ratio between upper and lower operation frequencies is larger than 2:1 in ultra wideband amplifiers [15]. This topology provides better return losses as well by arranging transistor sizes, like unequal-sized FETs [16].

The purpose here is to sum all output powers in phase by arranging drain lines together with drain capacitance and gate lines with gate capacitances. Transistor gate and drain parasitic capacitances are embedded within matching transmission lines to satisfy in-phase summation. Figure 2.4 shows a schematic example for distributed matching to show what this matching look like [16]. Achievable frequency bandwidth is the highest in this topology with respect to harmonic reaction and reactive matching. Despite of return loss and bandwidth advantages, output power, gain and efficiency performances are limited. Especially GaAs distributed amplifiers can be used as first-stage driver amplifier in RF systems, not as a power amplifier at the final stage. Recently, GaN technology is also commonly used in distributed amplifiers. Thanks to GaN technology power density advantage, higher output power can be achieved [17]. Even with this power improvement in distributed amplifier, they have still lower output power, gain and efficiency with respect to reactive matching amplifiers. Another disadvantage of this matching is that it needs complex small and large signal true models. It's difficult to obtain complex transistor models with high accuracy even at large signal operations. An example layout is shown at Figure 2.5, which is a 2-18 GHz 11 W GaN MMIC distributed amplifier [17].

The third and the final matching topology discussed in this part of the thesis is reactive matching. This matching is used at high power and high efficient amplifiers. Achievable bandwidth ratio for this matching type is up to 3:1 which is lower than distributed matching and larger than harmonic reaction matching. Since two or three stage circuit structure is possible for this matching type, larger gain and higher output

power than distributed amplifier can be obtained [18]. However, perfect input and inter-stage matching cannot be satisfied. Therefore, lower return loss and gain ripple performance are occurred with respect to distributed matching topology. This matching type is made up by LC (inductor-capacitor) high and low pass filters. An example MMIC layout is shown at Figure 2.6 which 2.5-6 GHz RF MMIC amplifier [19]. Due to high gain, output power and efficiency requirements, this reactive matching topology is chosen from all three options in this thesis. Also, it's believed that 3 times bandwidth requirement can be achieved with this reactive matching topology.

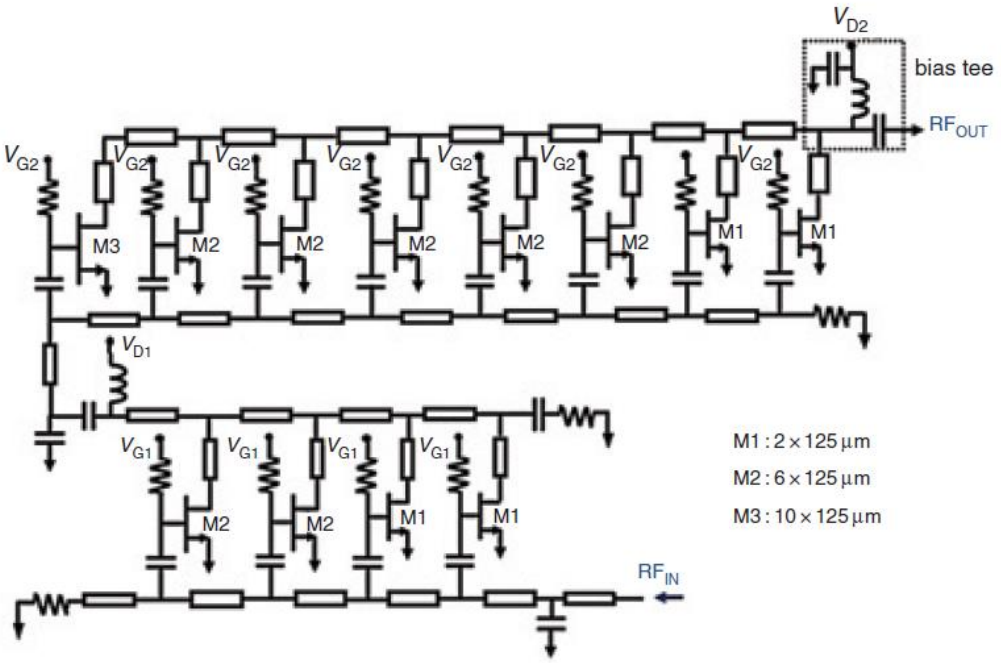


Figure 2.4. Schematic of a distributed matching amplifier [16]

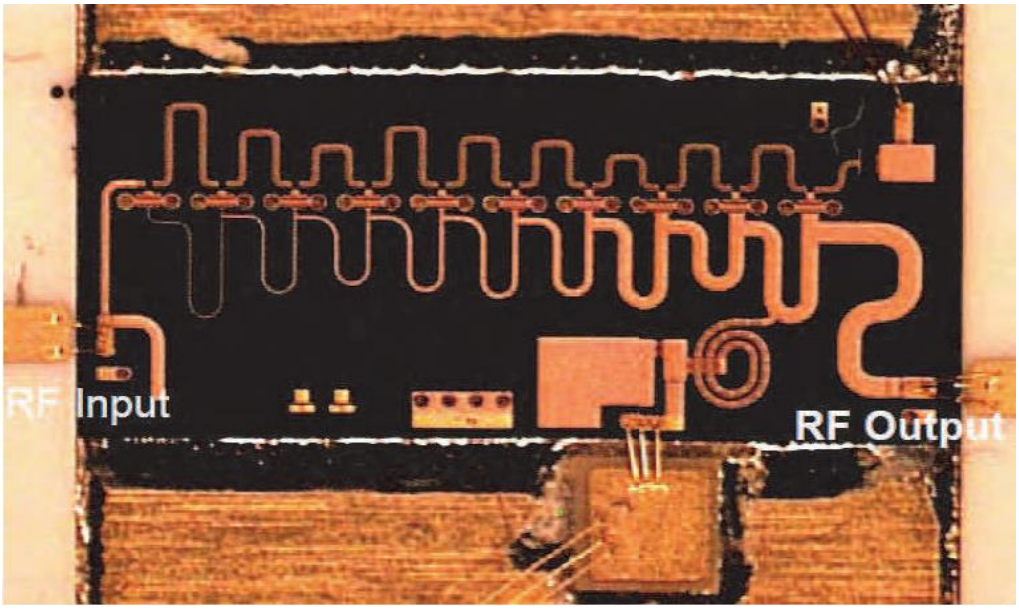


Figure 2.5. Photograph of the 2-18 GHz 11 Watt MMIC amplifier [17]

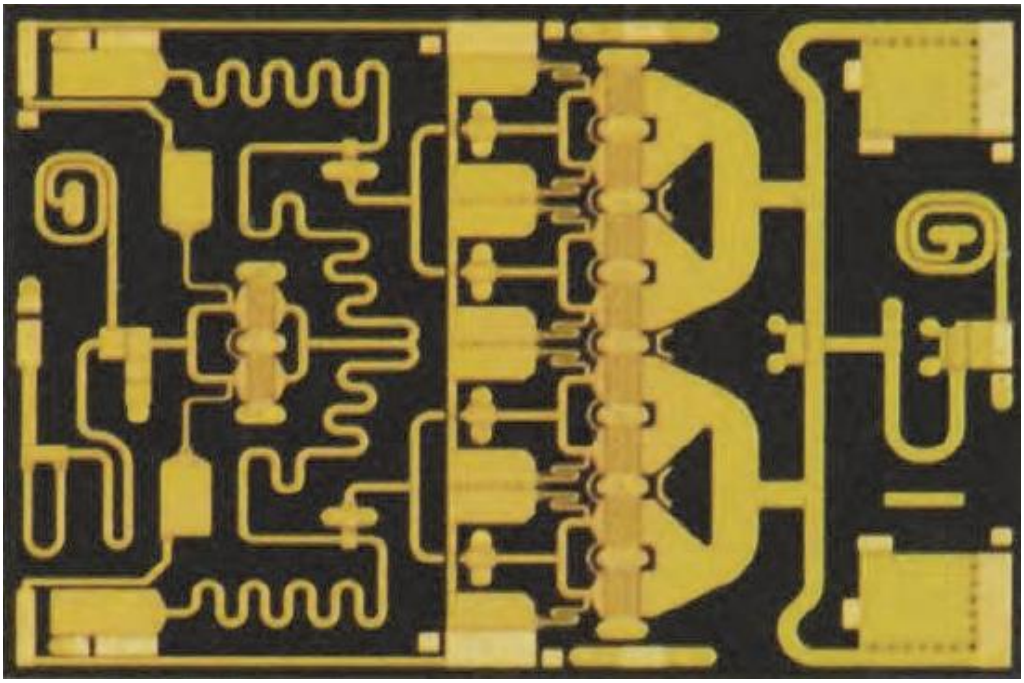


Figure 2.6. Photograph of the 2.5-6 GHz 30 Watt MMIC amplifier [19]

2.6. Design Procedure

In this part of the thesis, design procedure of an amplifier is discussed. First of all, design requirements such as frequency band, output power, gain and efficiency should be defined. Proper technology for MMIC should be selected for target performances. GaAs and GaN MMIC RF amplifiers are commonly used a lot in this RF MMIC area. If high output power and efficiency are needed at high frequencies, GaN process can be chosen. However, GaN process is much expensive than GaAs, it can be used if the cost is affordable. Then, transistor selection is critical for the design. Load-Pull measurements or simulations should be performed to chosen transistors to find optimum loads. Matching designs are performed to obtain optimum load and source impedances by considering layout as well. Output power and efficiency should be taken into account during simulations. Finally, electromagnetic (EM) simulation is performed and the circuit is getting ready to manufacture.

2.6.1. Technology Selection

Design of a RF MMIC amplifier starts by choosing the technology. By considering requirements of a circuit such as output power, efficiency and frequency, technology can be determined. GaAs and GaN are proper technologies if operation frequency is high, microwave frequencies and high linearity, high output power and high efficiency needed. These processes are also classified with respect to gate lengths. For example, 0.45 μm, 0.25 μm and 0.15 μm gate length process is used commonly for GaN MMICs. While smaller gate length used, higher frequency operation can be achieved with output power trade-off. 0.45 μm process is used for C and S band high power, around 100 W, amplifiers. 0.25 μm process is used from S band to Ku band, up to 18 GHz, and obtainable power is around tens of Watts. In this thesis, since the frequency of interest is 2-6 GHz and power is around 5 W, 0.25 μm process is chosen.

2.6.2. Transistor Size and Topology Selection

After choosing technology, next critical step is to determine transistor sizes and numbers of transistors used. All technologies have their output power and efficiency characteristics. For example, 0.25 μm GaN process used in this thesis have around 5 W/mm output power density. All circuit topology is pre-determined in this stage. First of all, output power transistor size and numbers of transistors used should be decided by concerning output power target. Then, it should be decided that how many transistor and stages are used in the circuit. Gain and efficiency targets are important during these decisions.

2.6.3. Load Pull

Matching circuits are designed with respect to optimum load and source points of transistors and other performance targets of the design such as gain and return losses. Therefore, load-pull measurements and simulations are another critical part of the design. Load-pull tests should be applied to chosen transistors. Transistors RF performance behavior with respect to impedance sweep at Smith Chart is investigated by Load-Pull measurements. In this step, first of all, bias point should be decided for target efficiency level. This defines the class of the amplifier and so efficiency of the design. Different bias points can be taken into account to observe transistor behavior in detail.

2.6.4. Schematic Matching Design

After load pull step, schematic design is performed by considering technology, transistors and load pull measurement results. At this step, manufacture company process design kit (PDK) which includes almost all component models and transistor measurements are used. Schematic design procedure is introduced step by step in this part of the thesis.

2.6.4.1 Transistor Stability Analysis

As a first step, transistors used in the design are analyzed for stability. This stability analysis is applied to single transistor, not to the whole circuit design. Also, this analysis is performed at wide range of frequencies rather than only operation frequency, like starting from DC to higher frequencies. The single transistor should be stable before starting to other matchings. For this stability analysis, Rollet's criterion is taken as a reference. K and μ factors should be larger than 1 to obtain stable transistor performance as mentioned at (2.1) and (2.2).

2.6.4.2 Output Matching Design

To achieve target performances from transistors, specific impedances should be satisfied at transistor drain and gate sides. Output power, efficiency and gain performances are related to these impedances seen from transistors. These impedances are determined by load-pull measurements mentioned previously in this thesis. Matching circuits are designed to provide these target impedances, such as maximum power, maximum efficiency or optimum of both.

Output matching design is the first matching step of this thesis work. The system operation impedance, generally 50 Ω, is converted to target impedance seen from drain output power transistors. Basically, transmission lines and metal-insulator-metal capacitors, which creates inductor-capacitor (LC) filters, are used in this design. Smith Chart is used to observe impedance change at each component. At each step, effect of the component should be analyzed. Not only impedance value, but also loss of the output matching is important. The transistor output power drops as much as loss of the matching circuit. Therefore, both impedance region and loss are considered together in this section. Final output power and efficiency values should satisfy the target of the work. This stage determines output return loss of an amplifier (S22) as well. RF-OUT pad and bond wires analysis should be added to this design stage. The component after the amplifier should be considered during this bond wire analysis specially to compare simulation and module measurements.

One matching section cannot be enough for broadband or ultra-wide band amplifiers [19]. The frequency bandwidth gets wider as the number of matching elements increases. However, this matching section should be limited because each section brings more loss. Bode-Fano criterion defines the achievable bandwidth for a related matching network [20]. When matching section number is getting larger, minimum achievable reflection coefficient (Γ_{min}) is getting smaller. Then achievable bandwidth is much higher than one section matching as seen from Eq. (2.7).

$$\text{BW} = \frac{\pi\omega_0}{RCln(\frac{1}{\Gamma_{min}})} \tag{2.7}$$

2.6.4.3 Inter-Stage Matching Design

After finalizing the output matching circuit design, inter-stage matching should be performed at multiple section reactive matching topology amplifiers. In this matching, one aim is to match power transistor small gate impedances to driver transistors optimum load impedances. Another consideration in this stage is the gain since this stage affects the gain value and ripple. Stability components, such as capacitor and resistor, are also added to this matching circuit. At this step, design is performed step by step like output matching. Impedance changes after each matching component can be analyzed by Smith Chart again.

2.6.4.4 Input Matching Design

Final stage of a reactive matching amplifier is input stage matching. At this stage driver transistor gate impedance is converted to system impedance. This matching determines the input return loss performance (S11) of the design. This stage also affects the gain like inter-stage matching. Therefore, both input return loss and gain are considered during the input matching. Like other matching stages, step by step impedance analysis is performed in the input matching as well. Stability components can be implemented to this stage as well. This stage design should include RF-IN

pad and bond wire effects like output matching. Height and length of the bond wires are determined with respect to previous component of the amplifier module.

2.6.5. Electromagnetic Simulation

For an RF system, all components should be analyzed by means of electromagnetic simulations. Material used in components are described in detail to the software and electromagnetic simulations are performed. Layouts of the components are obtained from schematic design. All matching circuits are simulated to achieve optimum schematic design results. After all electromagnetic simulations are done, design rule check is performed to check whether the whole design is producible or not. Then, MMIC design is manufactured.

2.6.6. Measurement

Final and another important step is measurement of the MMIC. All RF performances should be checked carefully. All measurement system should be calibrated to measure correct results. Manufactured dies can be measured on test fixtures or directly on wafer. Large signal characteristics can be analyzed on test fixtures. For this type of measurement, fixture characteristics should be considered carefully. For example, connectors, aluminum input and output lines losses should be taken into account. An example for test fixture is shown at Figure 2.8 [21]. While mounting the die on the test fixture, epoxy is chosen by considering thermal and electrical performances of the epoxy and test fixture properties. Also, off-chip components are mounted to achieve stable measurement.

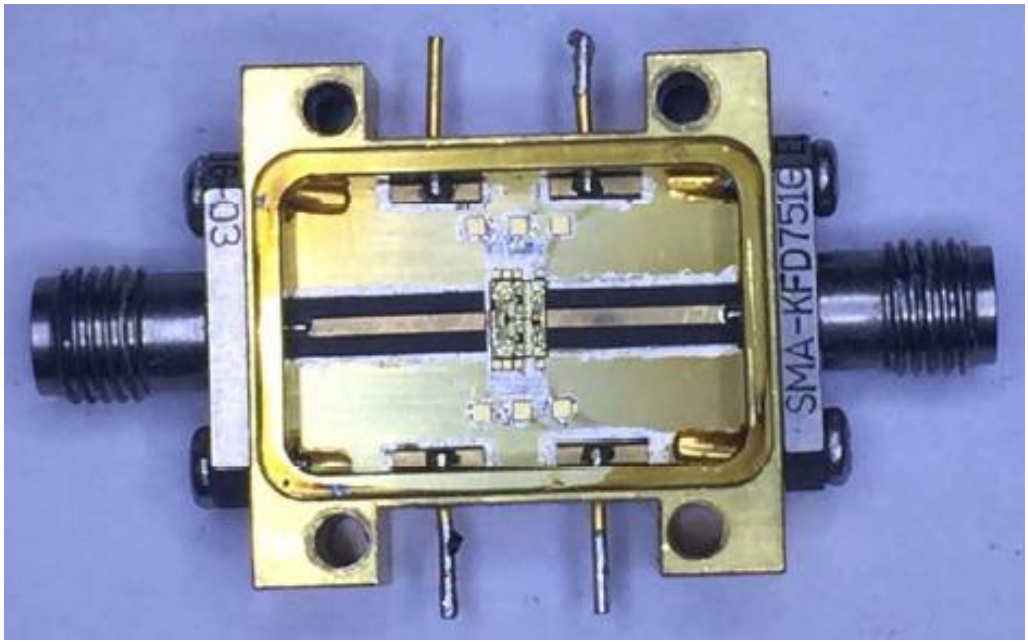


Figure 2.7. An example test fixture [21]

On-wafer measurements are much precise measurements. An on-wafer system provides an opportunity to measure directly from output and input pads of the MMIC.

CHAPTER 3

2-6 GHz GaN HEMT MMIC AMPLIFIER DESIGN

In this chapter, the 2-6 GHz GaN HEMT MMIC amplifier is introduced. All design steps are discussed in detail. The goal of this MMIC design is to achieve 5 W output power with 40% PAE and 30 dB small signal gain for 2-6 GHz frequency band operation. First, technology selection used in this MMIC design is described. Reasons to choose this technology and its details are explained. Then, transistor sizes and topology of the amplifier is determined. As the next step, load-pull measurements and simulations of selected transistors are performed in detail. Transistor performance behavior with respect to impedances swept at Smith Chart is analyzed, so that the optimum target impedances are found. After target impedances are determined, schematic design is performed to achieve RF performance targets. EM simulations are next step to be performed. All design parts are analyzed by EM simulations to be successful at first production. As final step, measurements are done on-wafer and on test fixture. Simulations and measurements are compared to observe the success of the MMIC design.

3.1. Technology Selection

As the first step, proper selection for the MMIC is chosen to satisfy system requirements. In this thesis, the goal is to achieve 2-6 GHz 5 W and 40% PAE performances. At microwave frequencies, GaN provides higher output power and efficiency than GaAs because of its wideband gap properties. Also, a requirement is to achieve those performances at small dimensions. For example, TGA2597 Qorvo 2-6 GHz GaN Driver Amplifier which is an example product for the thesis provides 1.5 W output power at 2.14 mm × 1.5 mm dimensions [22]. This means that TGA2597 has 1.5 W / 3.21 mm^2 ≅ 0.467 W/mm^2 power density. 5 W output target

at higher power density with low dimensions is quite challenging. Therefore, GaN process is chosen for this thesis. Despite the mentioned performance advantages, lack of linearity and high cost are the disadvantages of this process.

Since the operation frequency is 2-6 GHz and 5 W output power is needed, commercially available 0.25 μm GaN process is chosen as the gate length. Process design kit which includes most 0.25 μm GaN components models and manufacturing is provided by this company. This process products can be supplied with 28 V drain voltage which is a system requirement for this thesis. Output power density is given as at least 5 W/mm at 10 GHz for this process. The dies are produced at 4 inches wafers and the GaN/SiC substrate thickness is 100 μm. The process includes two different metal layers called MET1 (1.1 μm) and MET2 (4 μm). Inductors are generated with these metals together which provides high power operation. Capacitors also obtained by the dielectric between these two metals. There is a resistor thin film layer and resistors are generated by this layer.

3.2. Transistor Size and Topology Selection

At this step of the design, sizes of transistors and design topology are determined. Matching type is chosen as reactive matching which includes low and high pass filters, capacitors and inductors. Reactive matchings can provide higher output power and gain than distribute matching types. For broadband MMIC amplifiers, however, distributed topology is also used. It provides better matching response opportunity and less sensitivity to process change [23]. A disadvantage of distributed topology is high output power and especially high gain cannot be achievable for small size dies. For this reason, reactive matching topology is chosen for high gain, high output power and high efficiency even it's harder to perform broadband matching then distributed topology.

Next step is to determine transistor sizes and numbers. First of all, the MMIC needs to provide 5 W (37 dBm) output power and the 0.25 μm GaN technology has maximum 5 W/mm power density at saturation case. One 8×200 μm transistor is

chosen as output power transistor. For this decision, output matching loss and the loss causes mismatching from the optimum load point are taken into account. Since the operation band is broadband, optimum load may not be satisfied for all frequencies. When the matched load is not at optimum point, the transistor cannot provide maximum power, there will be loss. The calculation during this determination is given below:

$$8\times200\ \mu m \text{ transistor} = 1.6 \text{ mm device} \quad (3.1)$$

5 W/mm power density × 1.6 mm = 8 W = 39 dBm maximum output power (3.2)

Total loss = 1 dB output matching loss + 0.5 dB mismatched loss = 1.5 dB loss (3.3)

Achievable Out. Power = 39dBm max. out. power – 1.5dB loss = 37.5dBm (3.4)

As seen from Eq. (3.1) – Eq. (3.4), by 8×200 μm transistor 5 W output target power can be obtained. Small signal gain target is 30 dB and around 15 dB small signal gain can be obtained by one stage. Therefore, driver stage should be added to design to obtain 30 dB gain and drive the power transistor. If power transistor is saturated at 4 dB, it means that the transistor can provide 11 dB large signal gain. To satisfy 5 W (37 dBm) output power, the driver transistor should provide 26 dBm power for linear case. For the driver stage transistor, 6×90 μm transistor is chosen. Inter-stage matching loss is much larger than output matching, since gain is also a consideration and optimum gain loads are different than maximum power loads. Another reason is that there will be stabilization components like resistors which result higher loss.

$$6\times90\ \mu m \text{ transistor} = 0.54 \text{ mm device} \quad (3.5)$$

5 W/mm power density × 0.54mm = 2.7W = 34dBm maximum output power (3.6)

Total loss = 2dB interstage matching loss+1.5dB mismatched loss = 3.5dB loss (3.7)

Achievable Out. Power = 34dBm max. out. power – 3.5dB loss = 30.5dBm (3.8)

This calculation is performed for 4 dB saturated output power, but driver stage of the amplifier works fine if it works at linear region. Therefore, driver stage transistor

should be chosen for 4 dB larger than the target (26 dB). However, larger transistor cannot be chosen for the driver since, larger transistor means smaller gain and larger DC consumed power. This effects both efficiency and gain. It's critical to choose optimum driver transistor size, not larger or not smaller. At the end, 6×90 μm transistor is chosen as driver transistor.

To summarize this step of the design, 2 stages reactive matching topology is chosen with 1×6×90 μm driver stage transistor and 1×8×200 μm output transistor. Figure 3.1 shows the topology of the thesis design. This drawing of the topology is made up at Advance Design System (ADS) software.

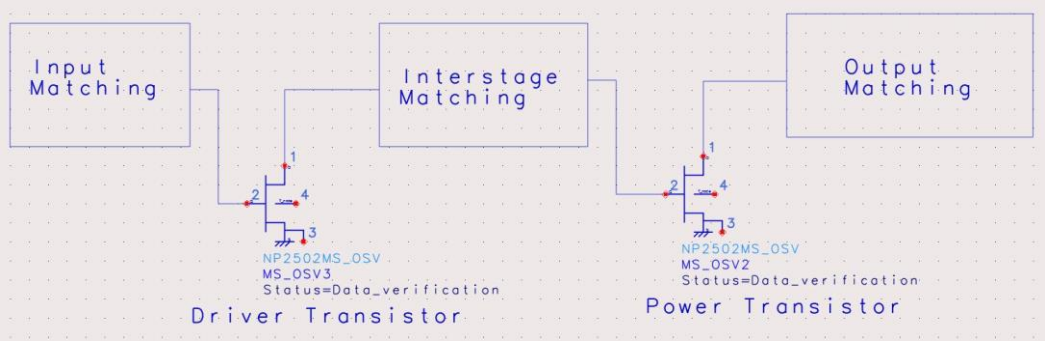


Figure 3.1. Circuit Topology Basic Schematic

3.3. S-Parameter and Load-Pull Measurements

After determining transistor sizes, S-Parameter and Load-Pull measurements are performed. Before measurements, bias condition is determined. Since the target of this study is high gain and high power with high efficiency, Class AB is determined as bias condition. This 0.25 μm GaN process operates at maximum 600 mA/mm current density. In this study, transistors are supplied with 100 mA/mm drain current (16% of maximum current) which is proper for Class-AB. Then, S-Parameters of transistors are obtained with the on-wafer probe station. For this measurements, Multiline Thru-Reflect-Line (M-TRL) calibration is used to obtain accurate measurement data. Calibration reference planes are moved to transistor drain and gate sides because of this calibration. These S-Parameter data of the transistors are

used at the rest of the design. Afterwards, load-pull measurements are carried out. Figure 3.2 shows Load-Pull measurement result of an example on Smith Chart. The measurement is performed for 8×200 μm transistor at 2 GHz. Left side of the Figure 3.2 shows power contours with 0.1 dB step while right side shows efficiency circles with 2% steps. Maximum output power at 2 GHz is measured as 39.9 dBm. Maximum PAE is measured as 63% which is quite enough. This measurement is performed for all frequencies. The measurement for 6 GHz is also shown at Figure 3.3. Maximum output power at 6 GHz is measured as 39.6 dBm as expected (~5 W/mm). Maximum PAE at 6 GHz is measured as 48%.

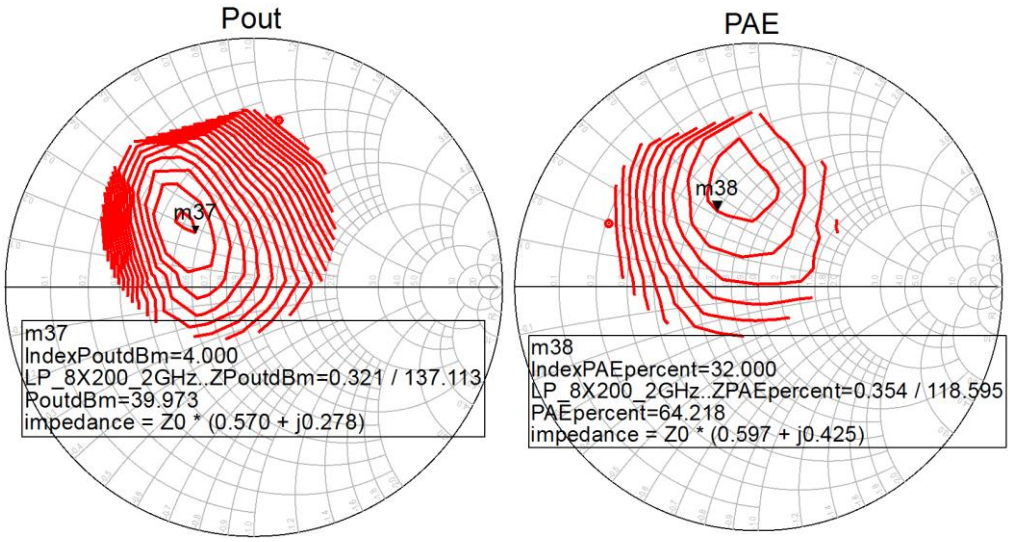


Figure 3.2. Load-Pull Measurement Result for 8×200 μm transistor at 2 GHz

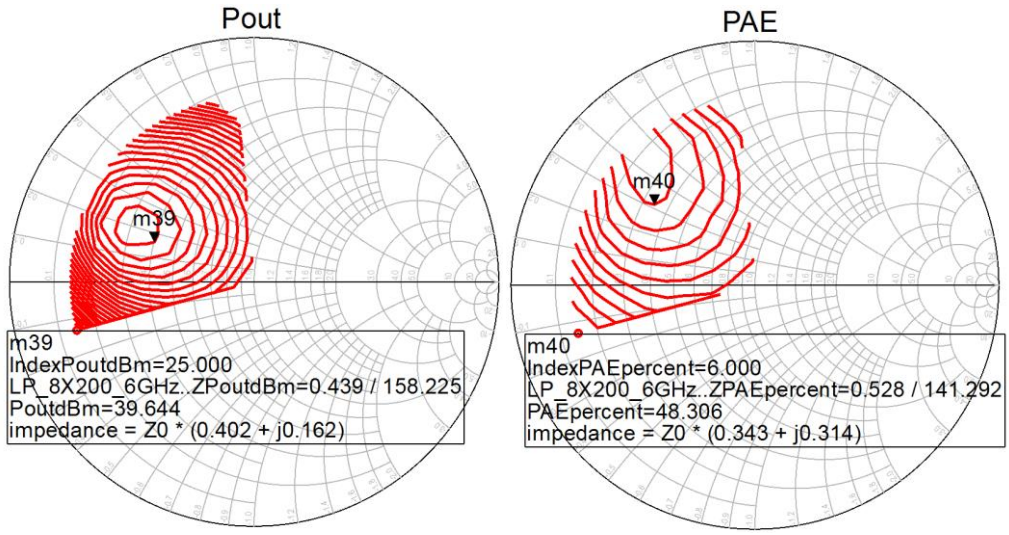


Figure 3.3. Load-Pull Measurement Result for 8×200 µm transistor at 6 GHz

This Load-Pull measurement is performed at on-wafer probe station with automated tuner. This automated tuner sweeps impedances at Smith Chart. It has two stubs inside and changes impedance by changing them. The tuner is controlled by a software which is provided by the tuner company. The whole system is calibrated and checked carefully to perform measurement correctly. The measurements are performed directly from gate and drain of transistors with launchers. Launchers are calculated during calibration and inserted into measurement by the software. An example setup for on-wafer probe station is shown in Figure 3.4 [24].

For the driver transistor 6×90 µm load-pull measurement is performed by simulation at Advanced Design System (ADS) software. ADS is used for all other simulations as well at this thesis. 8×200 µm transistor is manufactured before, therefore it can be analyzed by measurement setup. The driver transistor, however, is produced new and load-pull is performed at software. It is checked later by measurement as well. Since the driver transistor optimum loads don't effect as output power transistor, PDK large signal model can be used for driver stage. Also both measurement and simulation is carried out for this driver. Figure 3.5 shows the load-pull simulation result for 6×90 µm at 2 GHz. Blue circles show the power contours and red circles show PAE contours at the Figure 3.5.

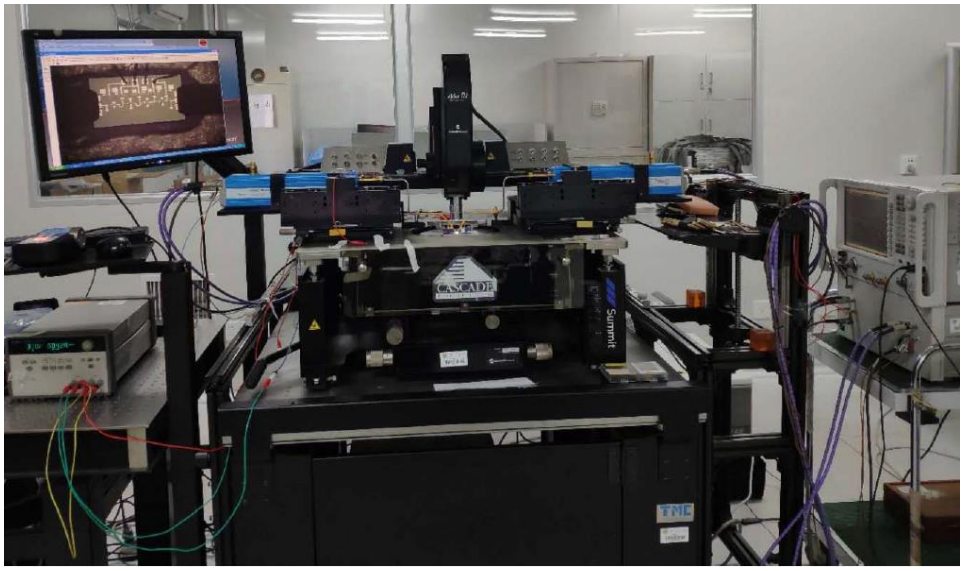


Figure 3.4. An example of On-Wafer Test Environment [24]

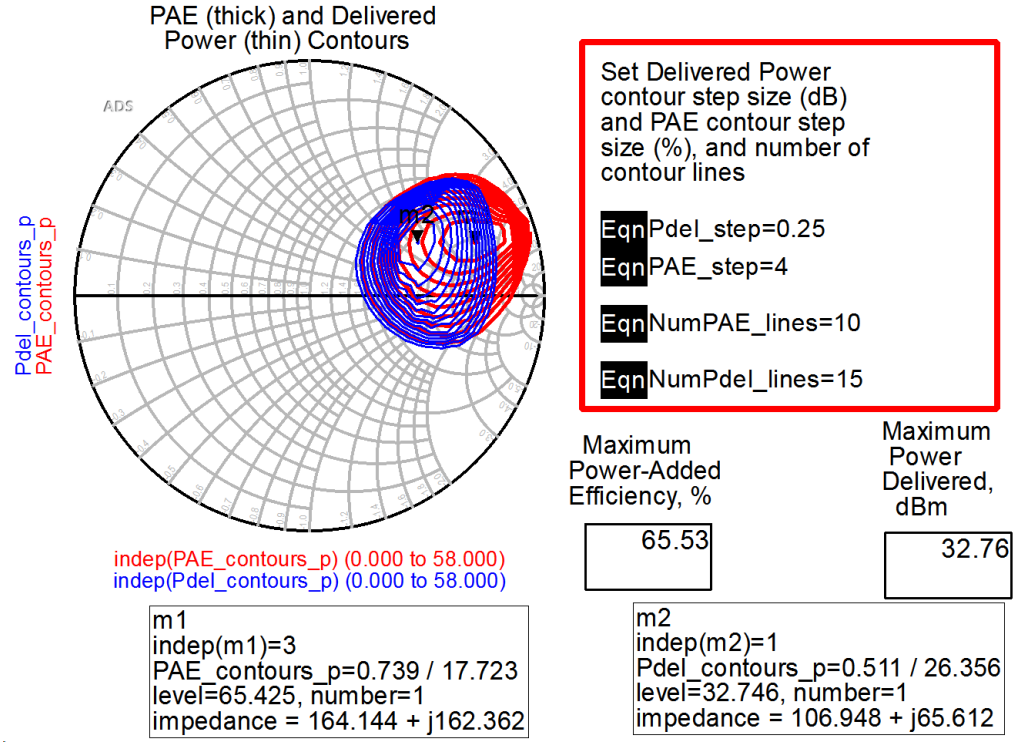


Figure 3.5. Load-Pull Simulation Result for 6×90 µm transistor at 2 GHz

3.4. Schematic Matching Design

3.4.1. Transistor Stability Analysis

Before starting matching step of the design, the used transistors should be analyzed to check stability. Rollet's criterion is used during this analysis. Besides Rollet's criterion, stability circles and 'μ' are also checked. As seen in Figure 3.6, transistor without any protection is normally unstable. Stability circles are inside of the Smith Chart and 'μ' is smaller than 1. These parameters mean that the transistor is unstable without any protection. Mu and Muprime should be larger than '1' [2]. If a load intersects with the stab circle, which inside of the Smith Chart now, the circuit shows unstable characteristics.

To have stable transistor operation shunt RC and series LRC networks added to the transistor gate. These components reduce the maximum available gain, but improves stability performance. Figure 3.7 shows the stability circuit components in the simulation and Figure 3.8 shows the stability analysis results after these components. 'μ' and 'μ′' is larger than 1 from 0.1 GHz to 10 GHz. Stability circles are at outside of the Smith Chart anymore. Therefore, transistor is stable due to RC and LRC networks added. During this analysis S-Parameter measurement is done for the 8×200 μm transistor. Not only load-pull, S-Parameter measurements are also performed for all transistors and they are used in the design. This makes first production success easier. Stability tools used in ADS is showed at Figure 3.9. Thanks to these stability tools, stability analysis is performed effectively.

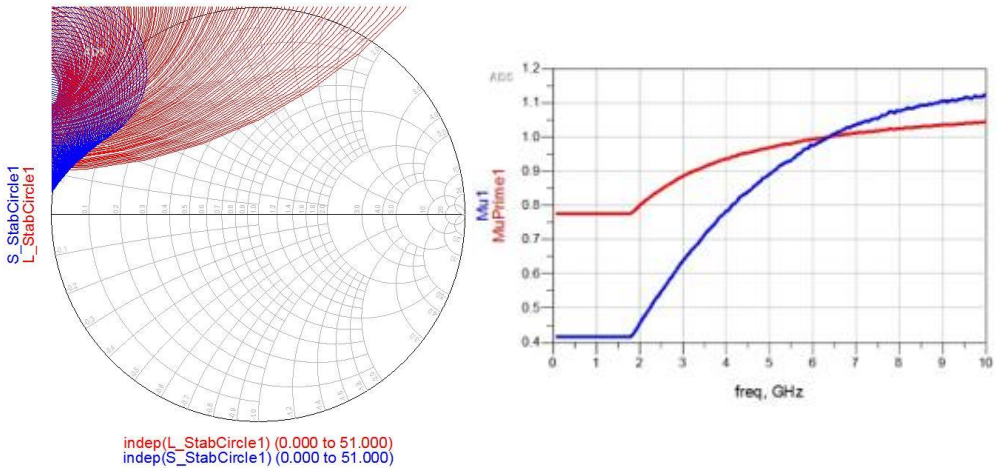


Figure 3.6. Stability Analysis of the transistor without protection

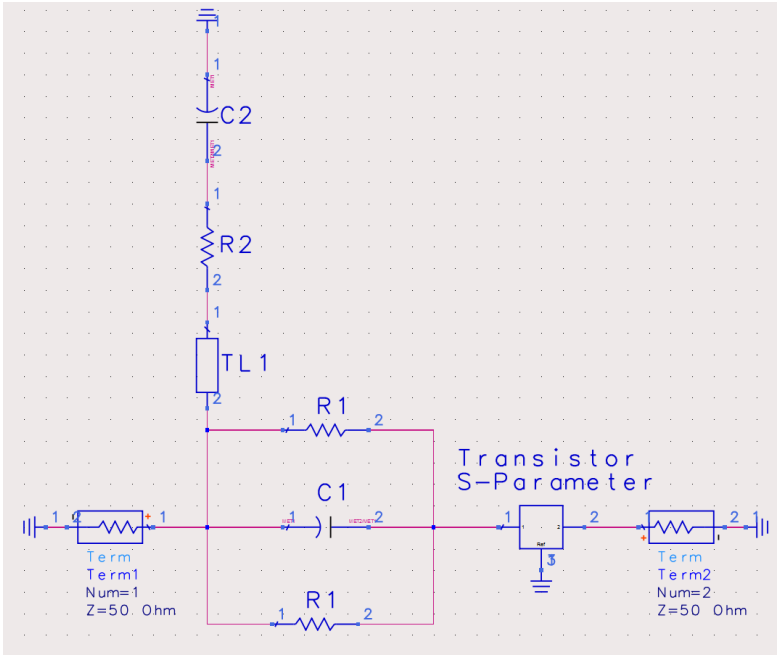


Figure 3.7. Stability Analysis Circuit of the transistor with RC and LRC circuits

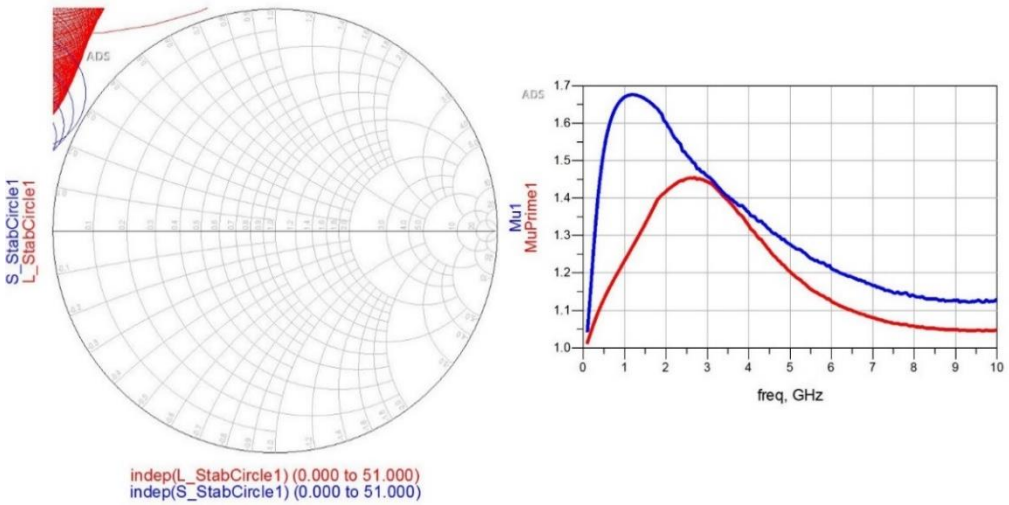


Figure 3.8. Stability Analysis Result of the transistor with RC and LRC circuits

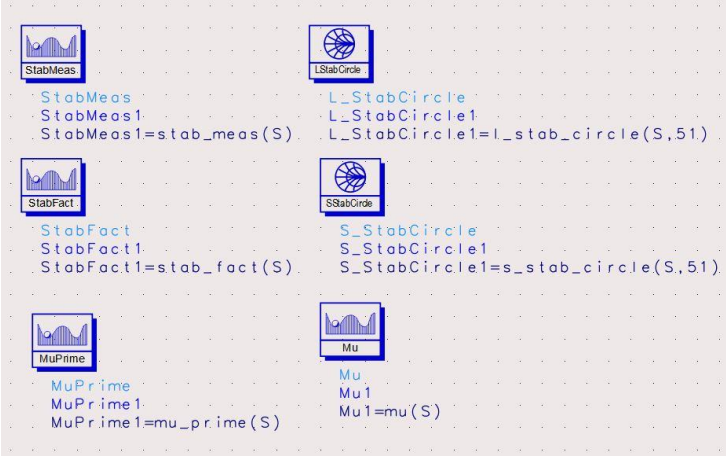


Figure 3.9. Stability Analysis Tools at ADS

3.4.2. Output Matching Design

In this section, output matching design is performed. The aim of this stage is to satisfy the matching from 50 Ω RF-Out system impedance to optimum loads of the power transistor. During this design, more than one matching sections are used to achieve the broadband matching.

Figure 3.10 shows a capacitor layout. In that layout it can be seen a backvia as well. The capacitor is shunt connected to a line and ground connection is satisfied by the

backvia. Figure 3.11 shows a spiral inductor layout which is used a lot in the design. Figure 3.12 shows a thin film resistor (TFR) layout.

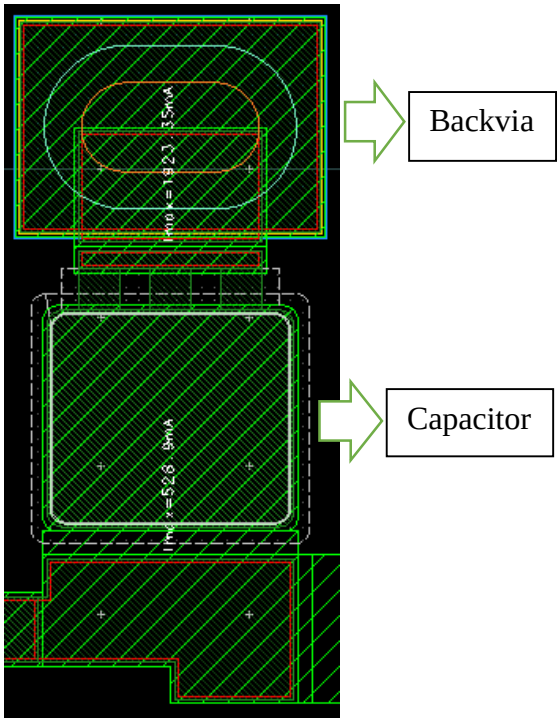


Figure 3.10. Shunt capacitor layout

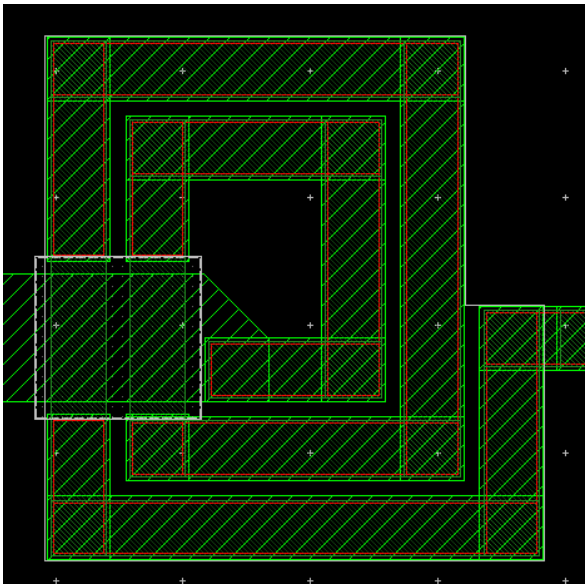


Figure 3.11. Spiral inductor layout

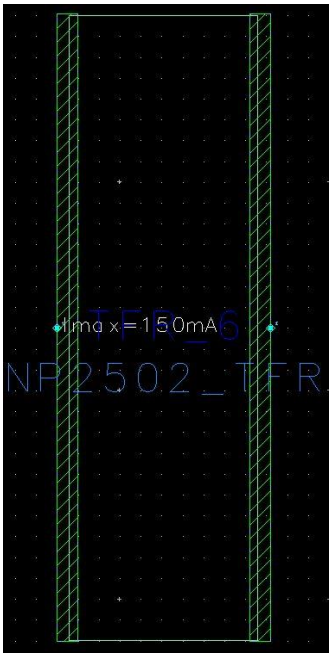


Figure 3.12. TFR layout

The matching is performed step by step. Every component effect is examined after adding to the circuit. Figure 3.13 shows the output matching circuit and Figure 3.14 shows how the matching circuit is analyzed step by step. Each added matching component changes the impedance on Smith Chart as shown in Figure 3.14. All components are selected and arranged carefully to satisfy optimum load targets. Output return loss and output matching loss are also additional concerns. Drain DC bias of the power transistor is also satisfied by this matching. DC bias line is added to this matching by considering current levels.

Since the size should be small, layout is also a concern during design, where y dimension is kept at 2 mm for output matching and x-dimension is kept at 1 mm, but the distance between RF-Out pad and power transistor is around 450 μm. Figure 3.15 shows the output matching circuit. Figure 3.16 shows the achieved output schematic result on the Smith Chart. At Figure 3.16, optimum power and efficiency load points are also shown to how good matching is performed. Output matching circuit loss and output return loss also shown at Figure 3.17. The loss is kept below 0.8 dB which is lower than 1 dB assumption.

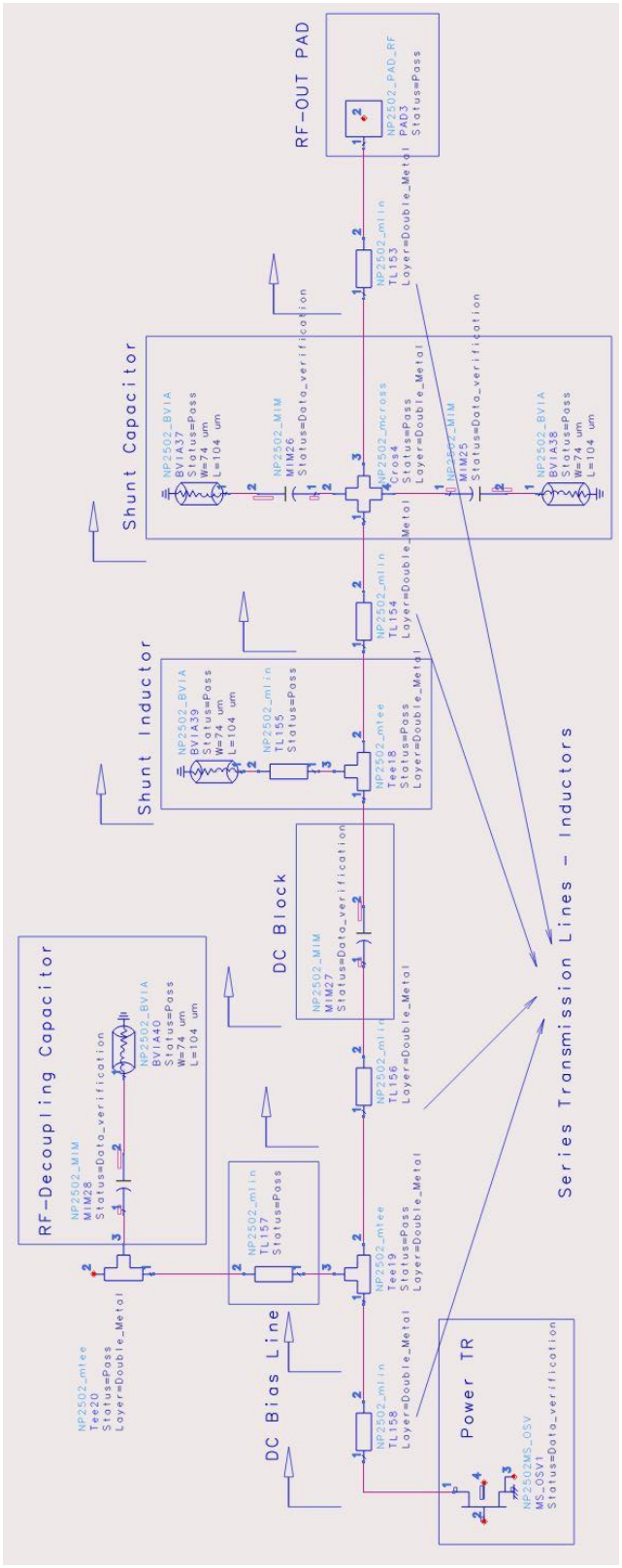


Figure 3.13. Output Matching Schematic Design

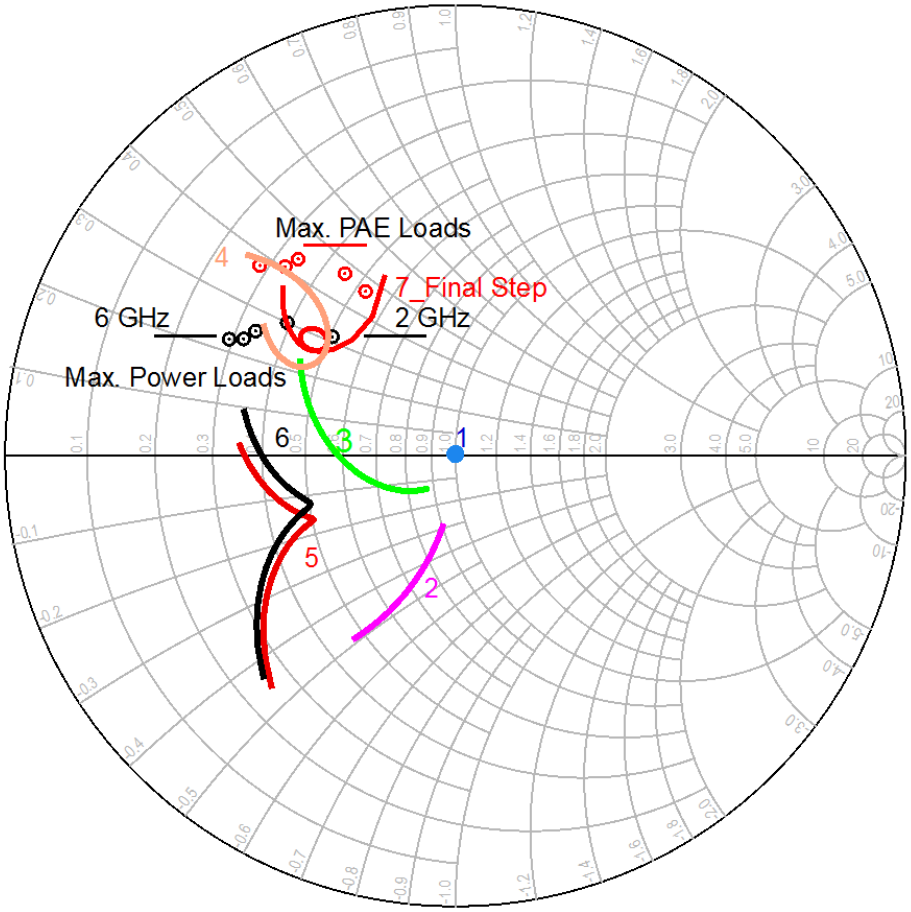


Figure 3.14. Output Matching Analysis Steps from 50 Ohm to Optimum Loads

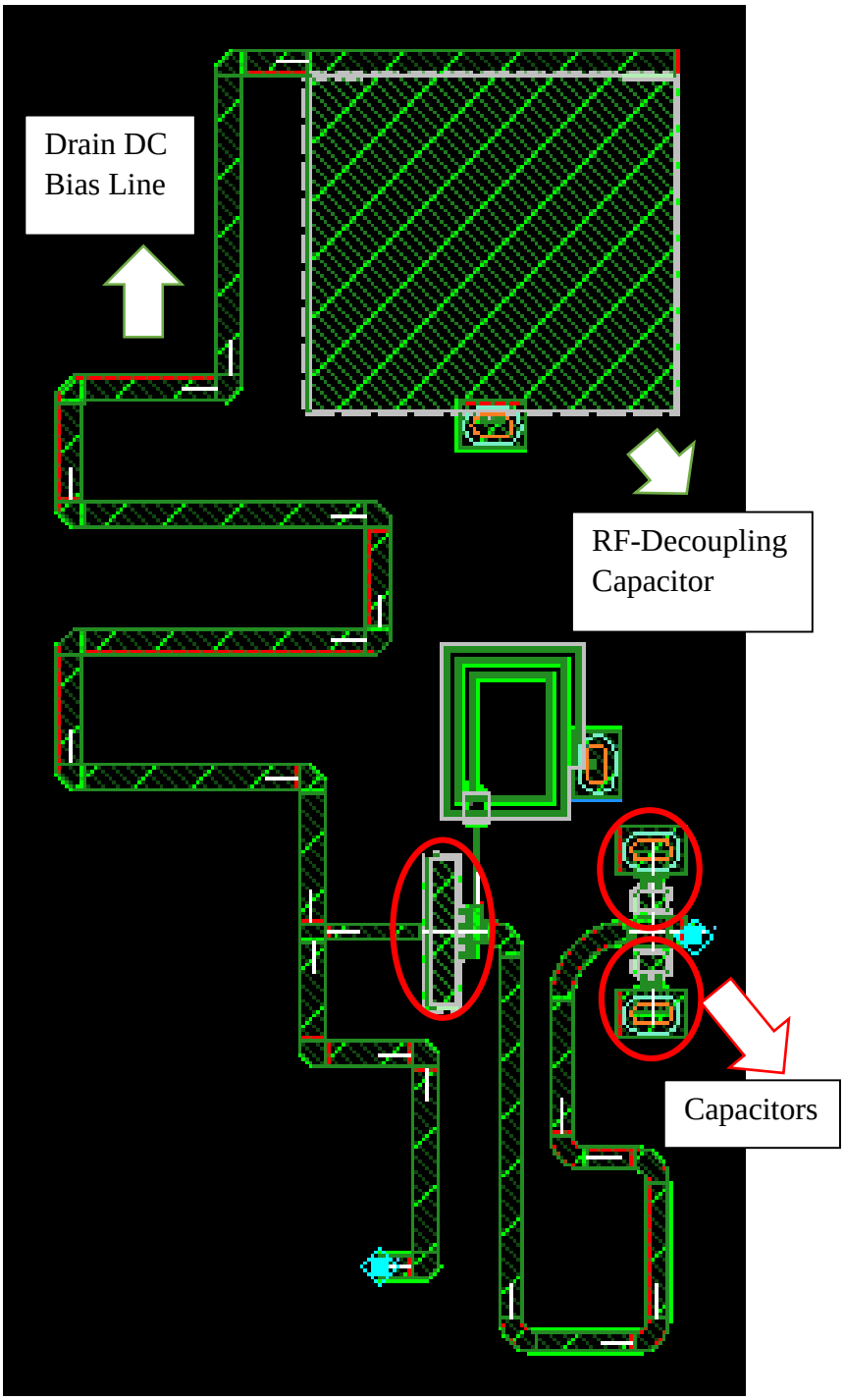


Figure 3.15. Output Matching Layout

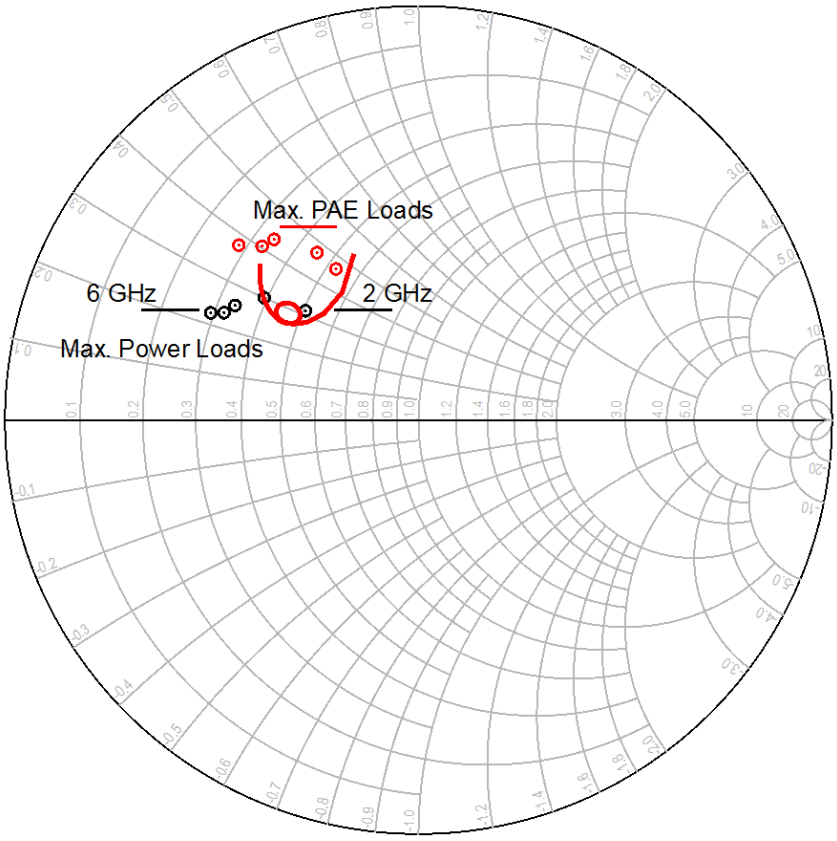


Figure 3.16. Output Matching Impedance Result with optimum power and efficiency load points

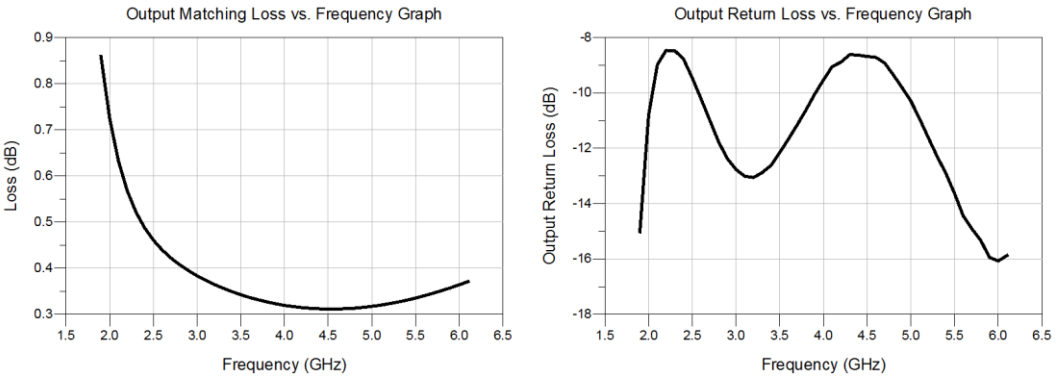


Figure 3.17. Output Matching Loss and Output Return Loss Results

3.4.3. Inter-stage Matching Design

The next step after output matching is the inter-stage matching. This matching satisfies impedance transition from the power transistor gate impedance to driver transistor optimum loads. Also, gain ripple and gain level are arranged by this inter-stage matching. At this stage, output power transistor gate DC voltage bias line and driver transistor drain DC voltage bias line are provided. First of all, shunt resistor and capacitor circuit (RC) is added to directly gate of the output power transistor to improve stability performance. In this circuit, RF signals from outside the operation band see the resistor and become lower. The signals inside operation frequency band passes through the capacitor which is nearly short at 2-6 GHz. Also, a line-resistor-capacitor (LRC) circuit is added to the gate for especially low-band stability. Not only these gate stability components, but drain decoupling capacitor is also added to the circuit. The inter-stage matching circuit is also performed step by step. Impedance is analyzed after each component. Figure 3.18 shows these impedance change steps. The whole inter-stage matching layout is shown at Figure 3.19. Simulated results for inter-stage matching is showed at Figure 3.20. The gain is not certain results because gain is adjusted with input matching as well. Therefore, fine tuning is done for whole circuit, this changes small signal gain and inter-stage matching.

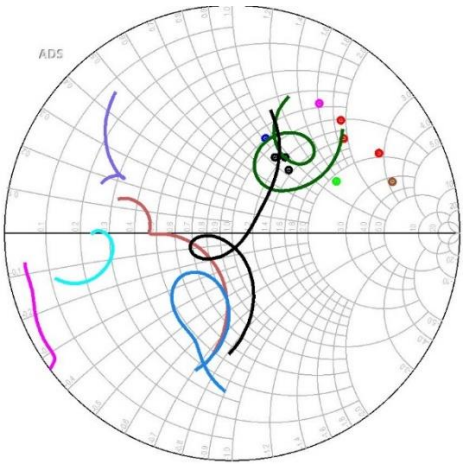


Figure 3.18. Inter-stage Matching Smith Chart Analysis for each components step by step

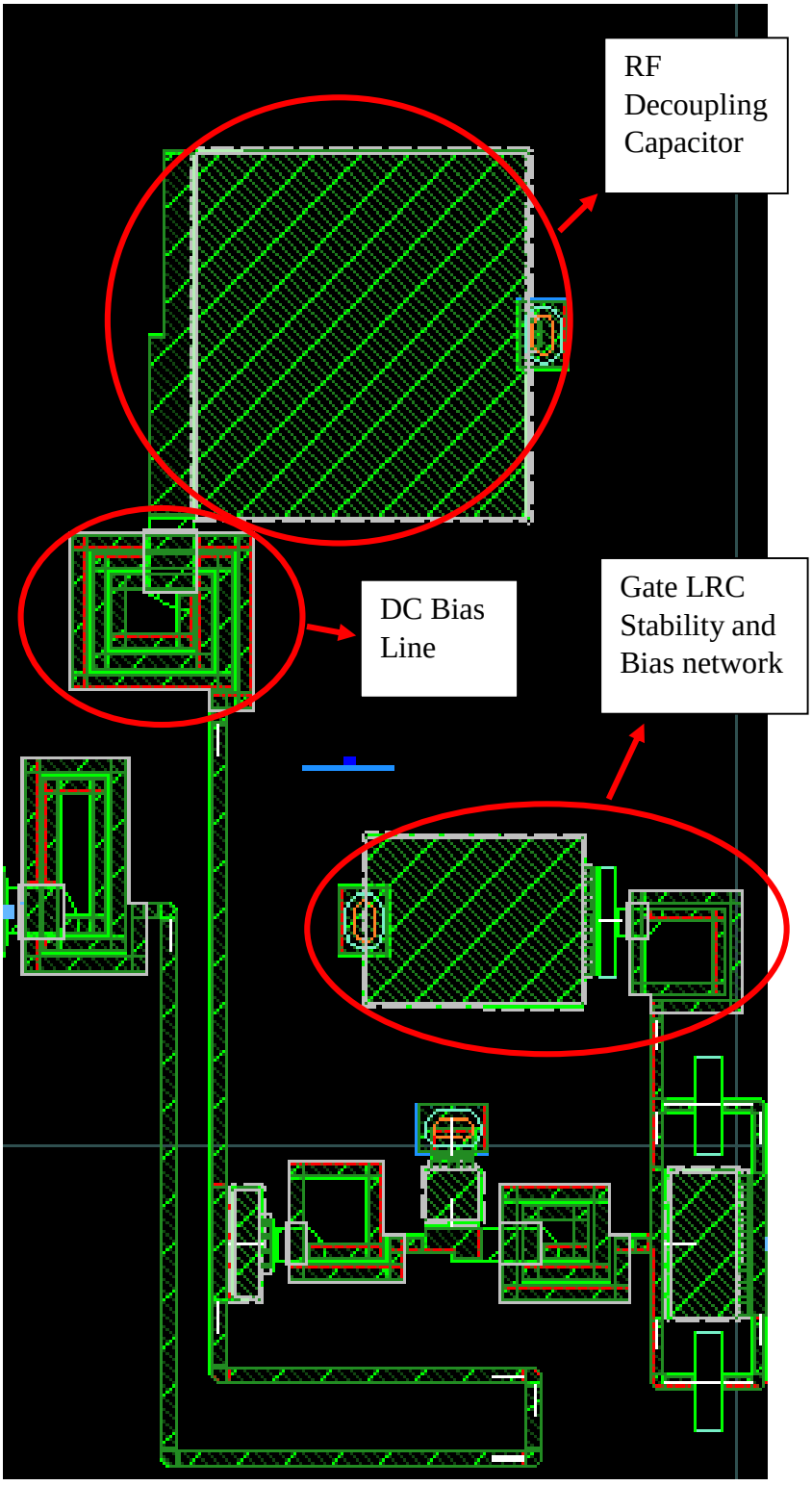


Figure 3.19. Inter-stage Matching Layout

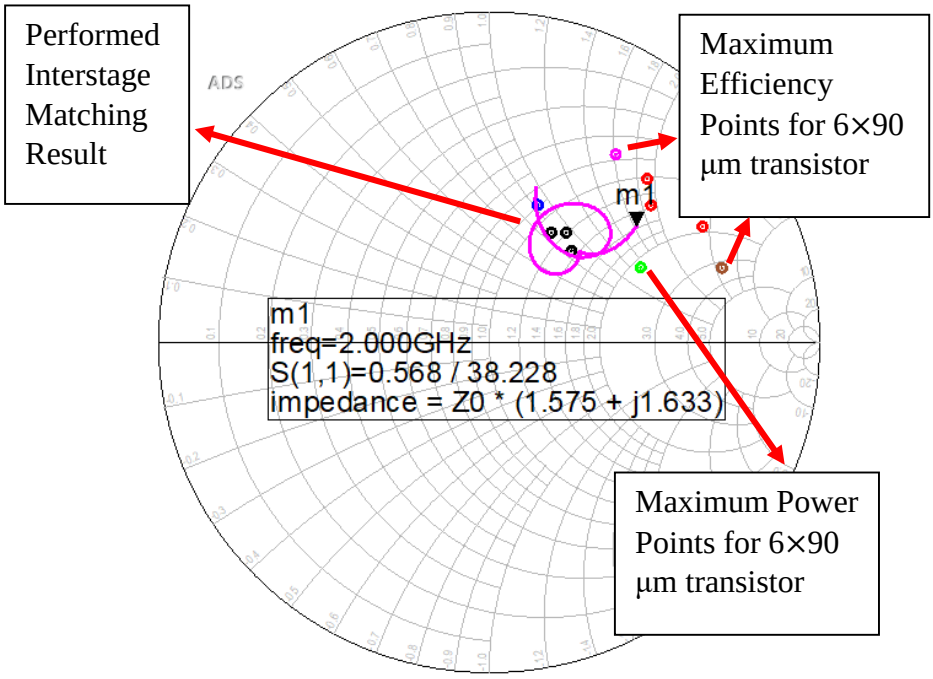


Figure 3.20. Inter-stage Matching Impedance Result

3.4.4. Input Matching Design

Input matching goal is to convert driver transistor gate impedance to 50 Ω RF-Input system impedance. Input return loss (S11), gain value and gain ripple are main considerations of the input matching. Figure 3.21 shows the input matching layout. RC and LRC circuit components are added to this matching as well to improve stability performance of whole design. The performance results are shown in Figure 3.22. These results are modified during EM simulation. Input return loss is below 15 dB which is good enough. Final small signal gain schematic design result is shown in Figure 3.23. This result is improved during EM simulations and better result is obtained. The gain is around 30 dB and gain ripple is around ±0.7 dB which better than the target.

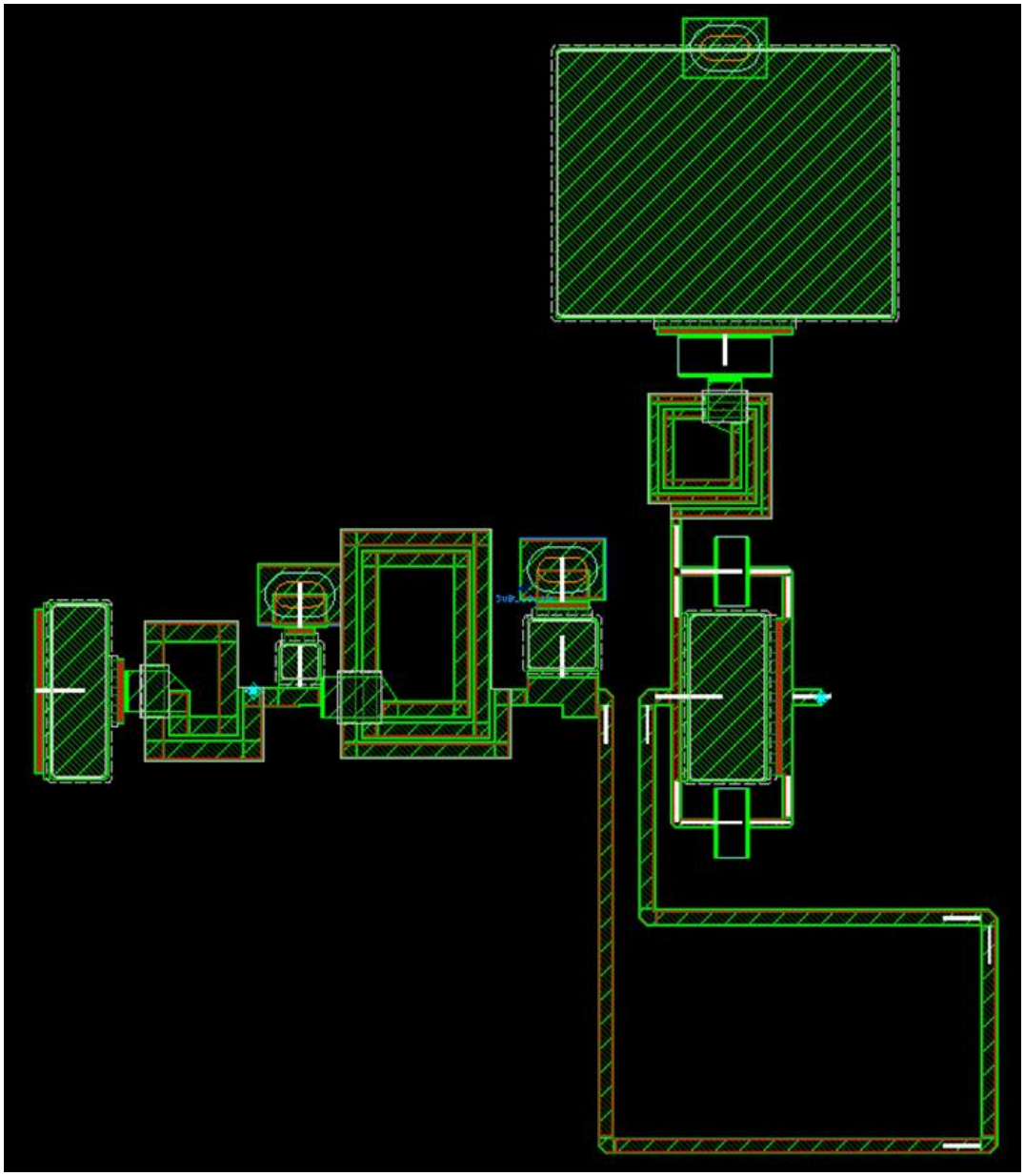


Figure 3.21. Input Matching Layout

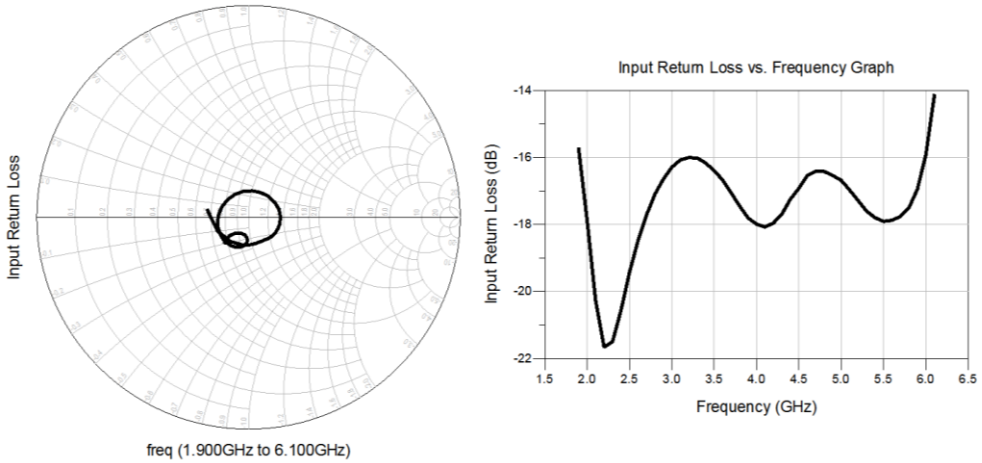


Figure 3.22. Input Return Loss Schematic Design Result

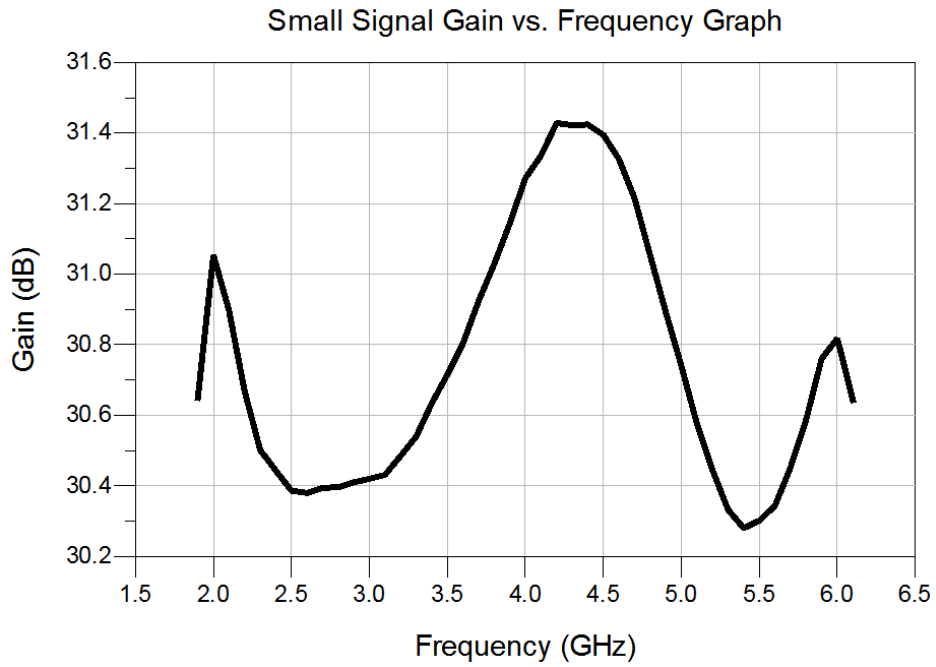


Figure 3.23. Schematic Design Small Signal Result

3.5. Electromagnetic (EM) Simulations

In this section, EM simulation results of the designed amplifier are presented. EM simulations of layouts obtained from schematic design are performed to achieve optimum results. For that purpose, an EM simulation model is designed first. Then, EM simulations are performed step by step again. Since EM simulations of entire matching stage take long time, they cannot be used for tuning directly. From the first components to whole matching design, EM performances are analyzed additively. These EM simulations are Method of Moments (MoM) analysis which only discretizes the metal interconnects to observe current distribution on the metal surfaces. MoM mesh structure is much smaller and simpler than FEM (Finite Element Method) [25]. It is compatible with layered stack up structures such as MMIC (dielectric and metal layers). Results of MoM simulations come out faster than FEM in ADS. Therefore, MoM simulation method is chosen for this design.

3.5.1. Output Matching EM Simulation

After obtaining schematic results, obtained output matching layout is analyzed step by step during EM simulations. Figure 3.24 shows the first and second parts of the output matching. Shunt inductor and series capacitor are added to first part to obtain second part. EM simulation result is symbolized and put into schematic and tuned to obtain same result with schematic design. An example for this EM result symbol is shown in Figure 3.25.

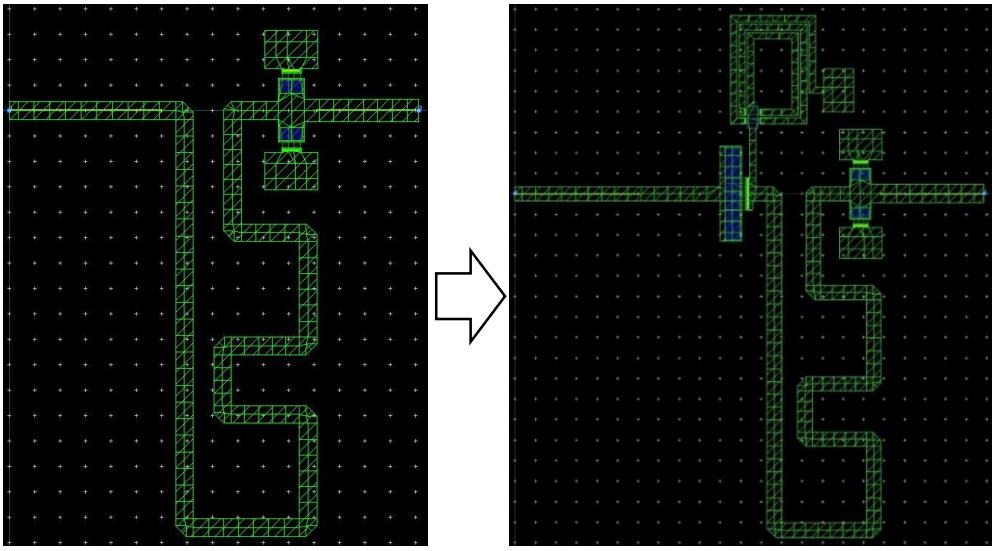


Figure 3.24. Output Matching EM Simulations (Part 1 is at left, Part 2 includes Part1 is at right)

Figure 3.25. Output Matching EM Part 1

Final output EM layout is shown at Figure 3.26. It differs a bit from schematic layout since EM and schematic simulations result different between each other. This output EM simulation impedance result is shown in Figure 3.27. As seen from Figure 3.27, output matching is satisfied for optimum loads. Matching impedance result is between maximum power and maximum efficiency points. An example case to show how this matching analysis is performed is given in Figure 3.28 for 2 GHz. That Load-Pull simulation results are for 2 GHz, red circles stand for output power and

blue circles stand for PAE. 2 GHz results is close to optimum power impedance and optimum PAE circles. This analysis is repeated for all single frequencies in 2-6 GHz with 1 GHz steps. Output return loss (S22) and output matching loss are also concerned during EM simulations and results are shown at Figure 3.29 and Figure 3.30 respectively. At 2 GHz, the loss is quite higher than rest of the operation frequencies. The good thing is that the matching load is at exactly maximum achievable power point for 2 GHz. After 3 GHz, the output matching loss is lower than 0.5 dB which is fine for broadband amplifier. Also, output return loss is lower than -8 dB which satisfies the target. Since the optimum impedances are away from 50 Ω, perfect output return loss cannot be satisfied. Therefore, this obtained output return loss is acceptable for this kind of amplifier.

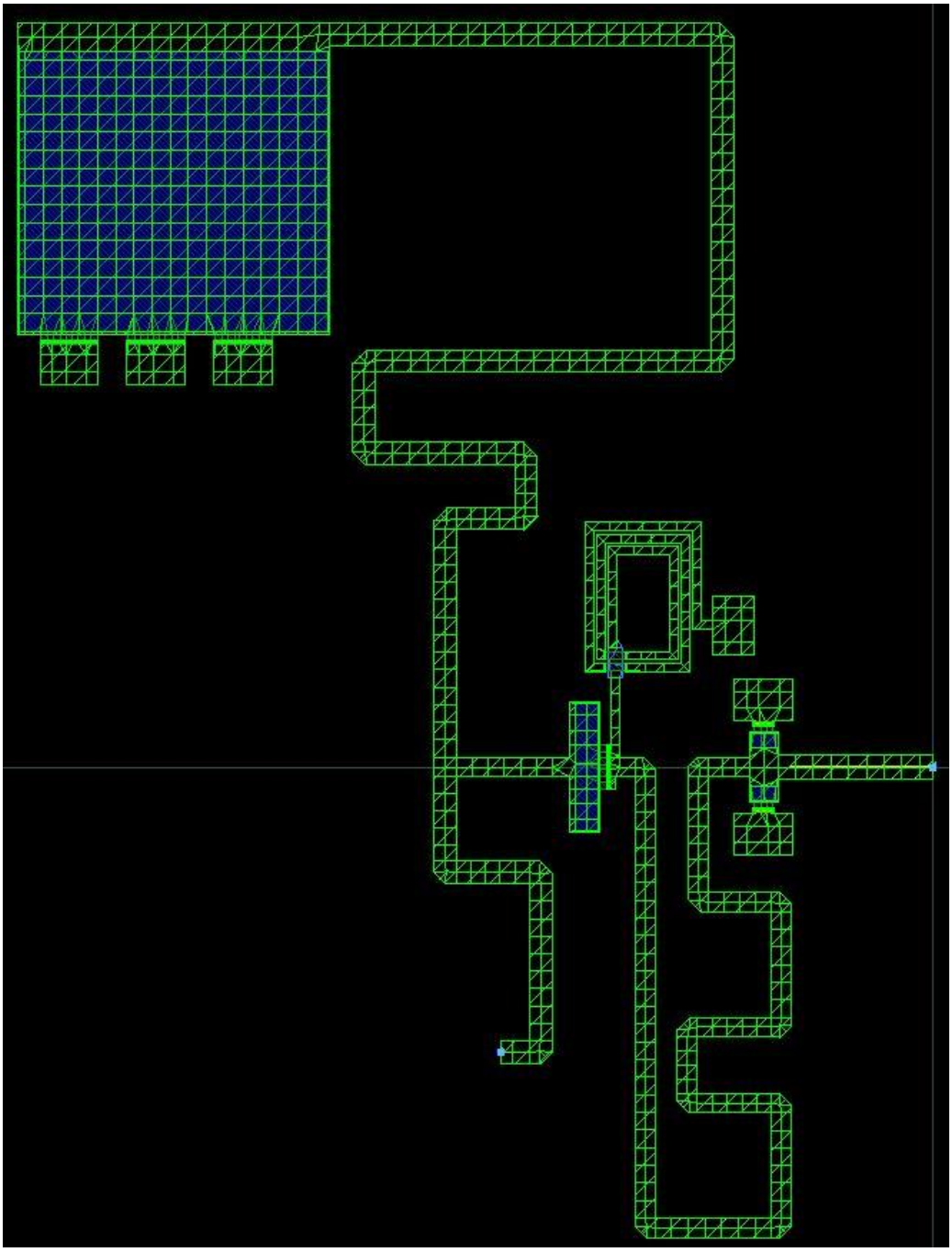


Figure 3.26. Output Matching Full EM Layout

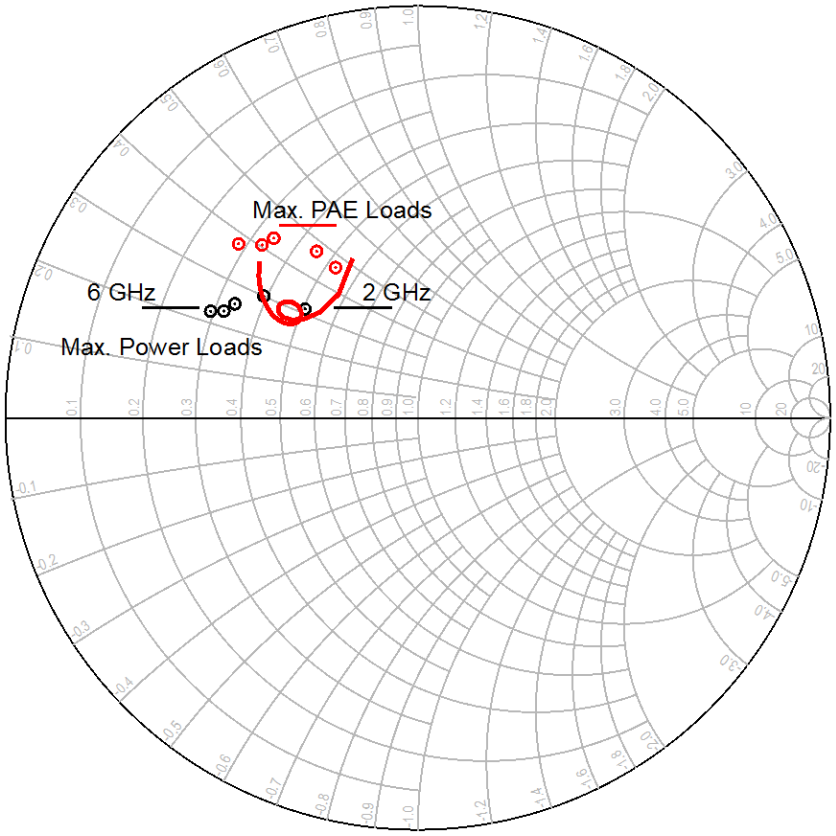


Figure 3.27. Output Matching Full EM Simulation Result

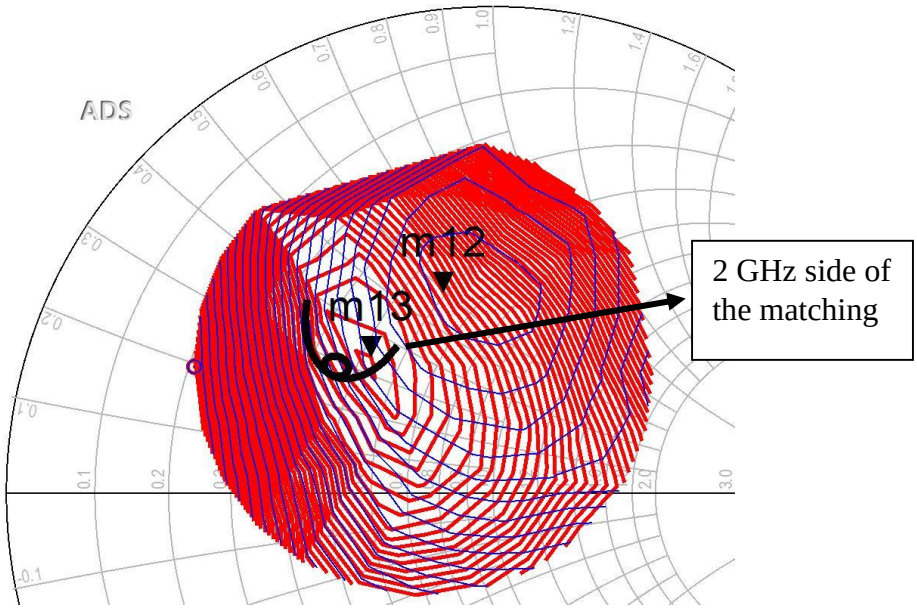


Figure 3.28. Output Matching EM Simulation Check for 2 GHz

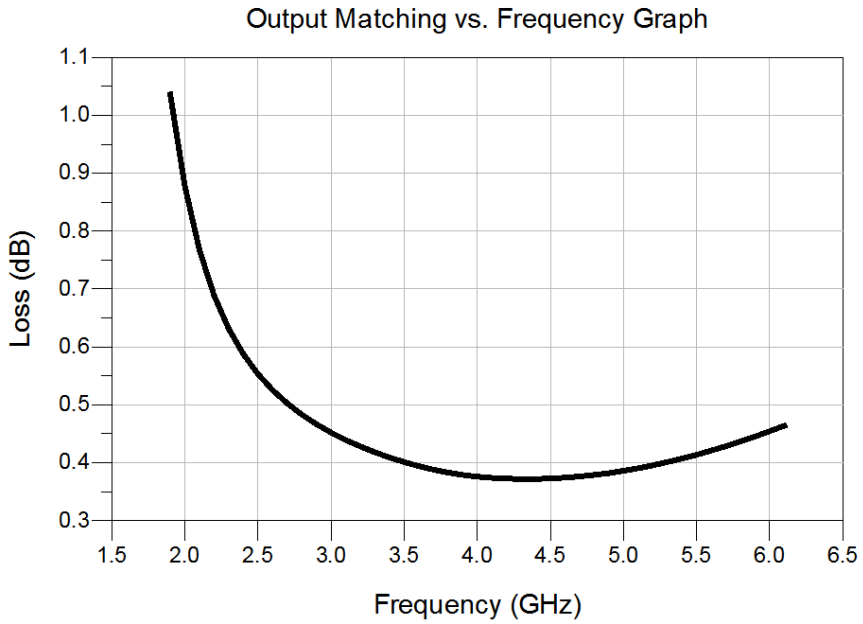


Figure 3.29. Output Matching Loss EM Simulation Results

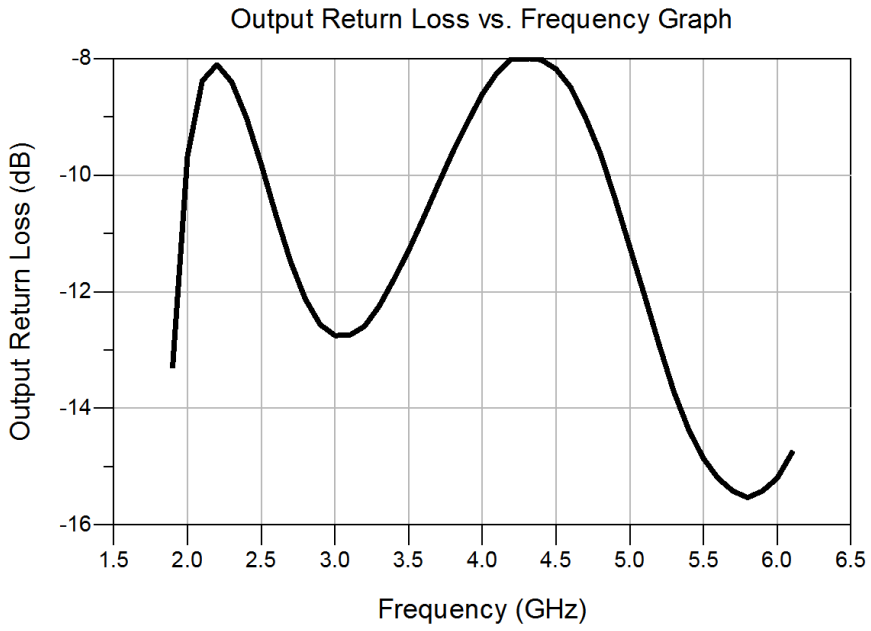


Figure 3.30. Output Return Loss EM Simulation Result

3.5.2. Inter-stage Matching EM Simulation

Next step after finalizing output matching EM simulations is the inter-stage matching. The same approach used in output matching EM simulation is applied to inter-stage matching. At this stage of matching, the aim is to drive the power transistor while concerning gain response. This means that matching is performed to reach optimum power and efficiency loads and to obtain high and flat gain response. Figure 3.31 shows the inter-stage matching impedance result. Simulations are performed at 1.9-6.1 GHz with 100 MHz steps for this matching analysis. Obtained result is close to optimum power loads whereas high and flat gain is achieved.

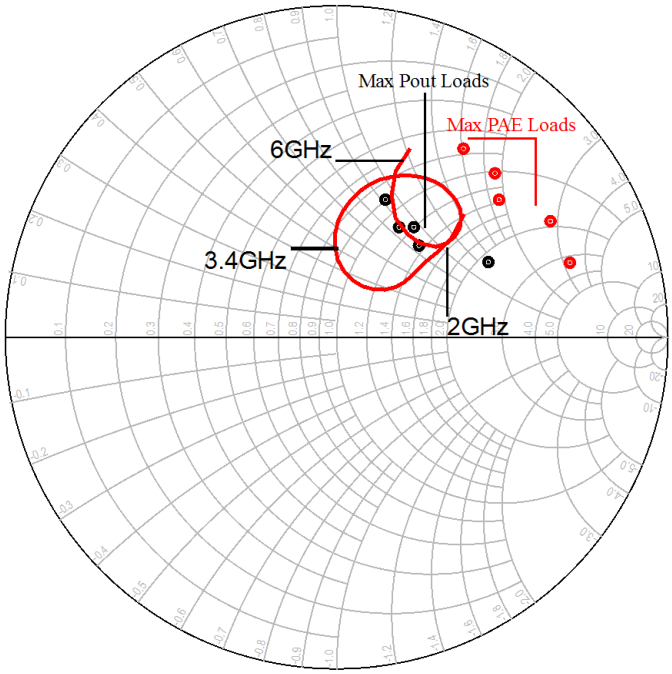


Figure 3.31. Inter-stage EM Simulation Impedance Result

RC EM structures show quite different results with the schematic, therefore layout of RC differs from the one given by the schematic. Figure 3.32 shows the inter-stage EM layout. Coupling between components are taken into account during EM simulations, so component's sizes can be modified. For example, drain bias line and last inductor of the inter-stage matching is coupled. This reduces their RF effects and both lines are longer than obtained at schematic to provide same RF performance.

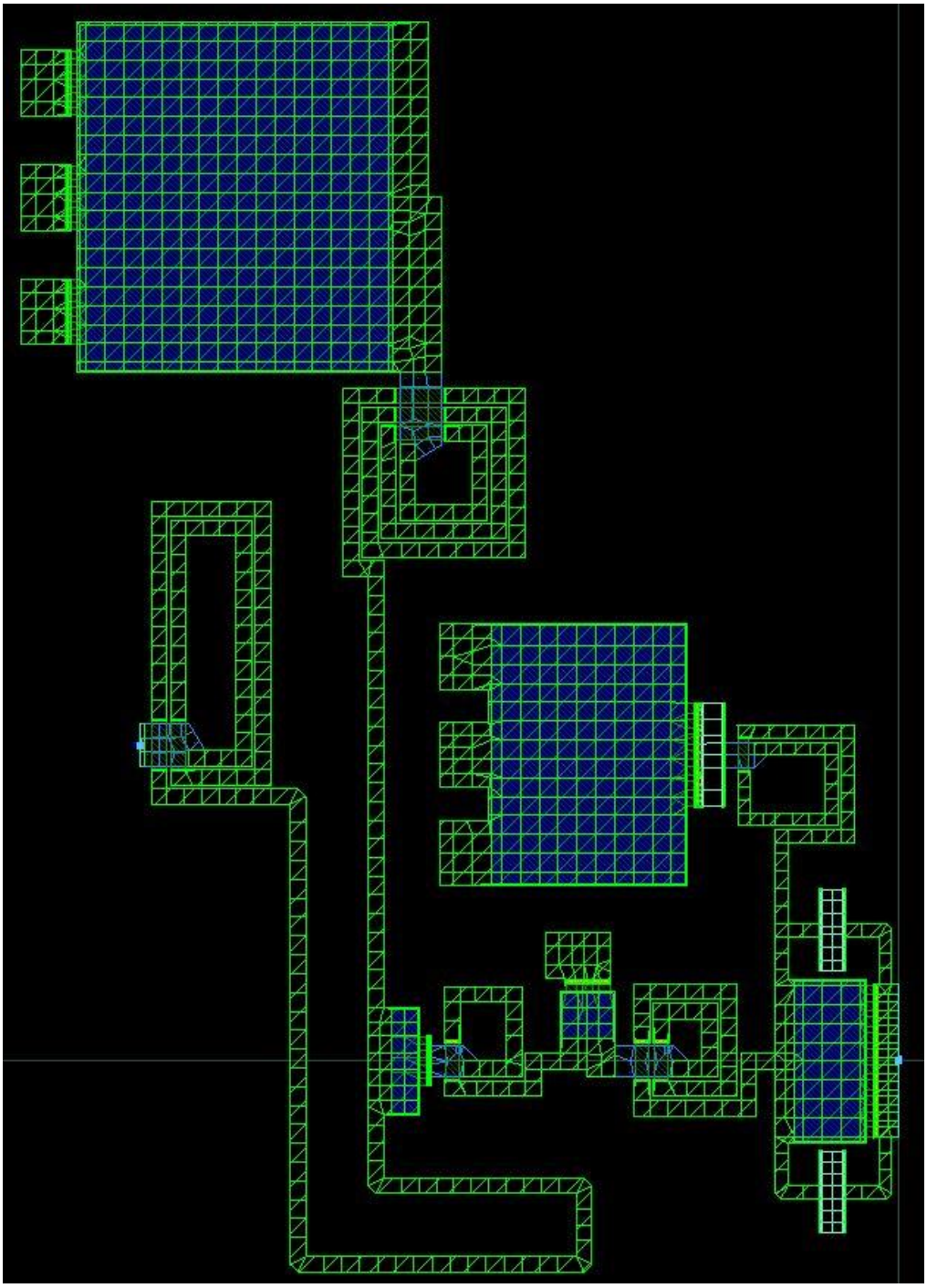


Figure 3.32. Inter-stage EM Simulation Layout

3.5.3. Input Matching EM Simulation

Final stage of the amplifier design is the input matching. EM simulations are performed to obtain optimum input return loss and gain results. RC structure is added to this stage as well to satisfy stability requirement. Figure 3.33 shows the input matching EM layout. This stage is also performed step by step to obtain same results with the schematic design. Chip size is another concern during this stage design. The stage is compressed to small region to have small chip size. Therefore, final layout of the input matching differs a lot from the first schematic input matching layout as shown at Figure 3.34. Successful results are achieved at this input stage EM simulations as shown at Figures 3.35 - 3.37.

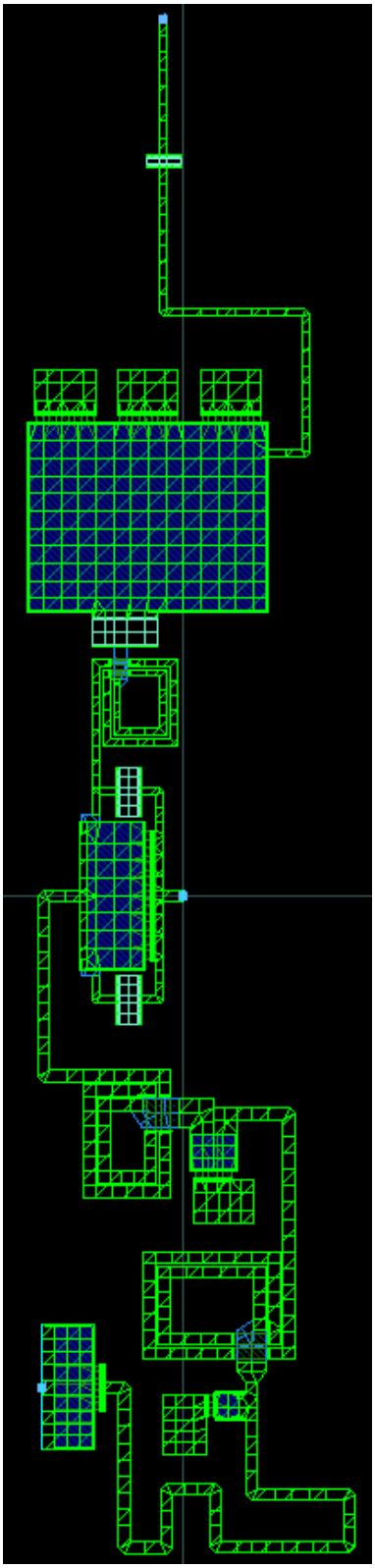


Figure 3.33. Input Matching EM Simulation Layout

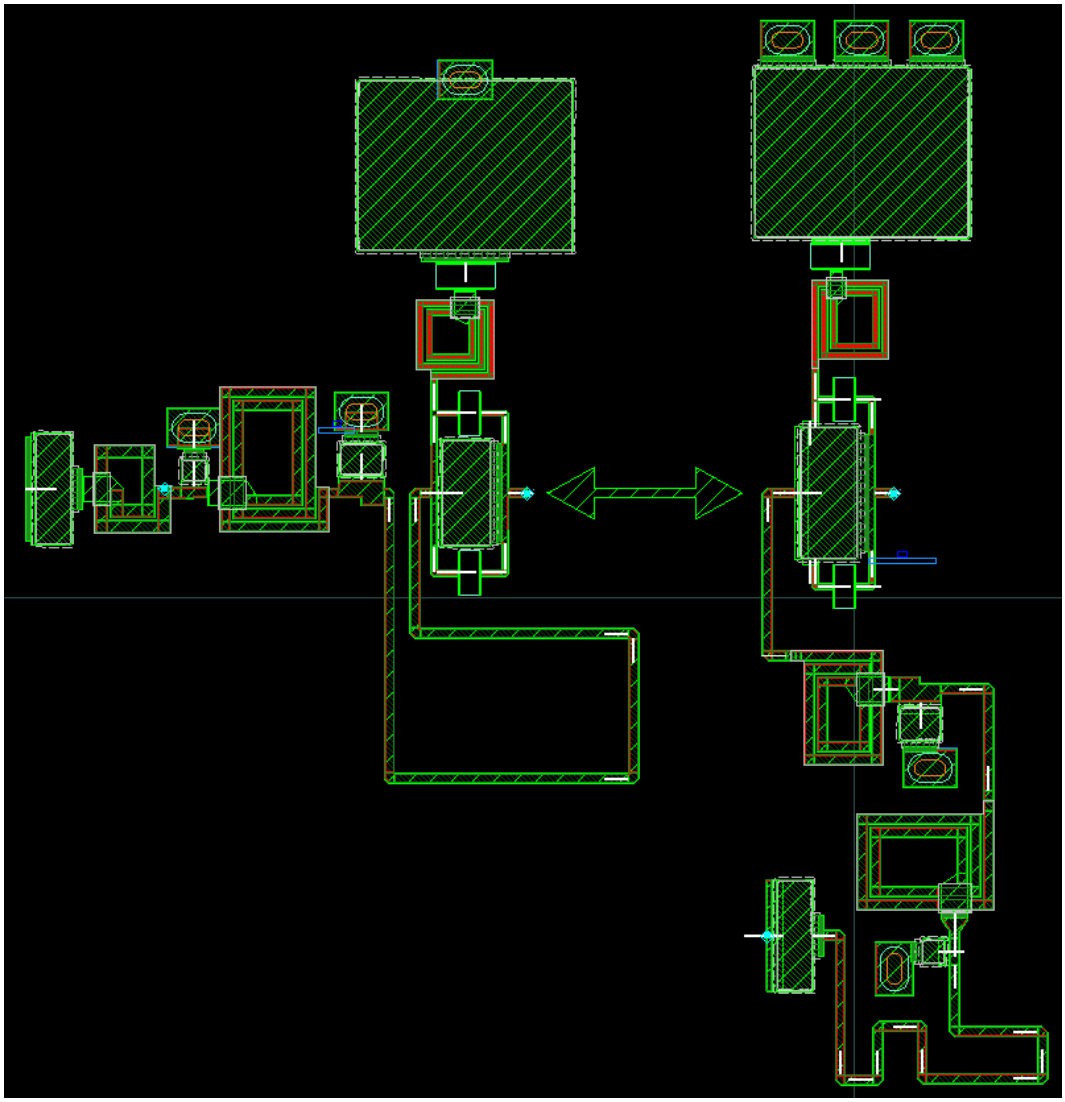


Figure 3.34. Input Matching Layouts Schematic Layout (left) and Final Layout (right)

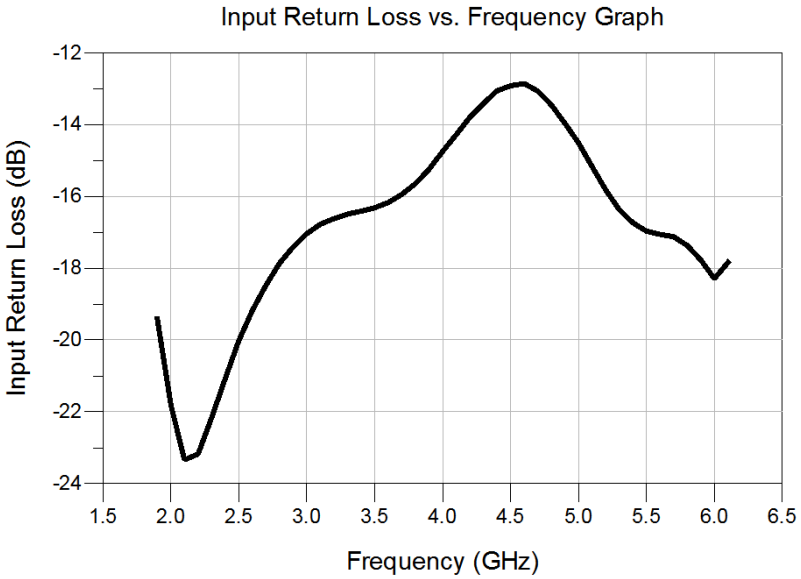


Figure 3.35. Input Return Loss EM Simulation Result

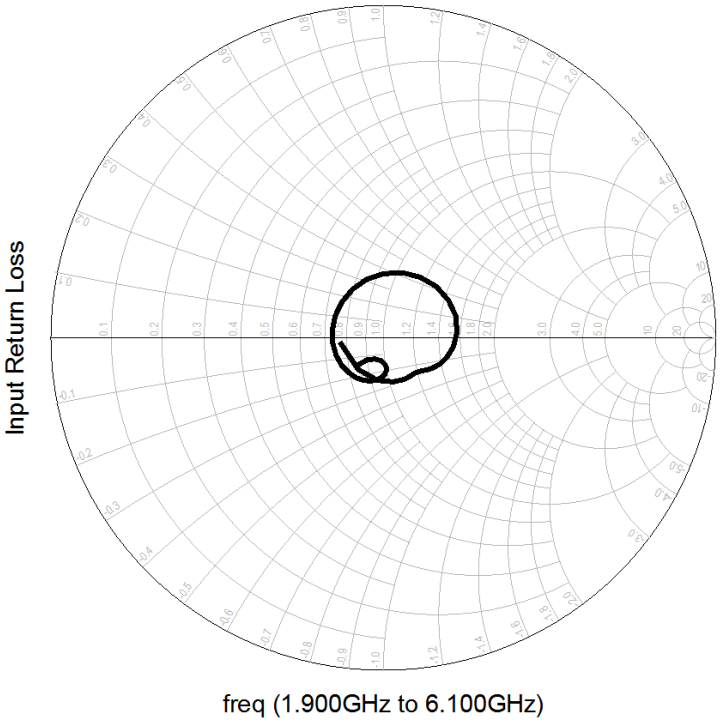


Figure 3.36. Input Return Loss EM Simulation Smith Chart Result

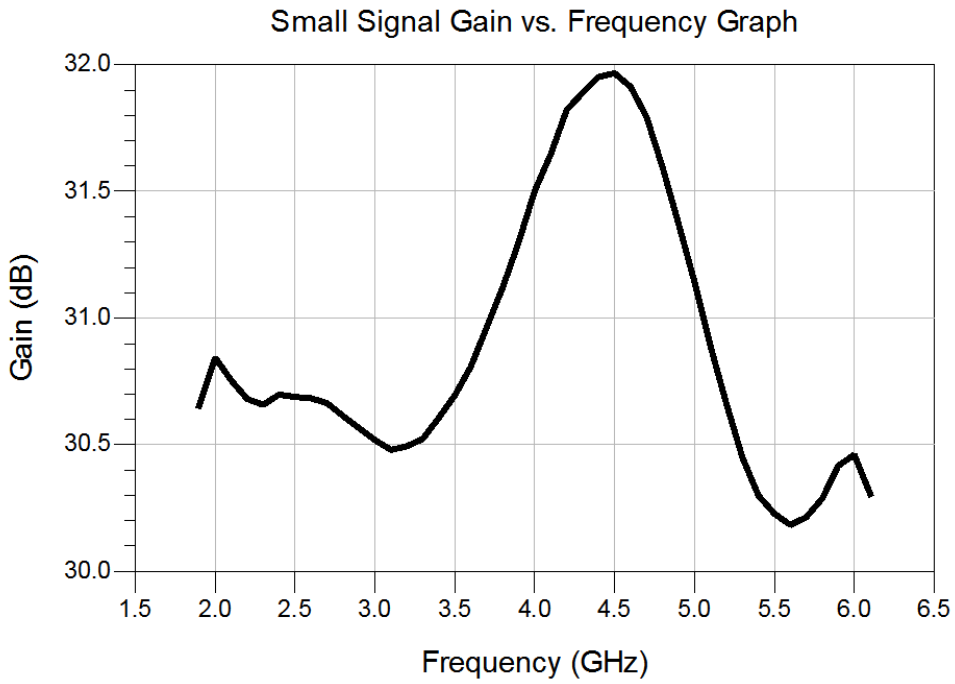


Figure 3.37. Small Signal Gain EM Simulation Result

In the previous sections of the thesis EM simulation results are performed separately. Input matching and inter-stage matching EM analysis are performed together as well to observe couplings between stages. This coupling between stages results as small change in the input matching. The capacitor of the input matching RC structure is increased a bit for fine tuning to obtain better results. The obtained results are shown at Figures 3.38 - 3.40. Red lines are separate EM analysis results while blue ones are obtained by performing stages EM analysis together. The layout for this EM analysis is shown at Figure 3.41.

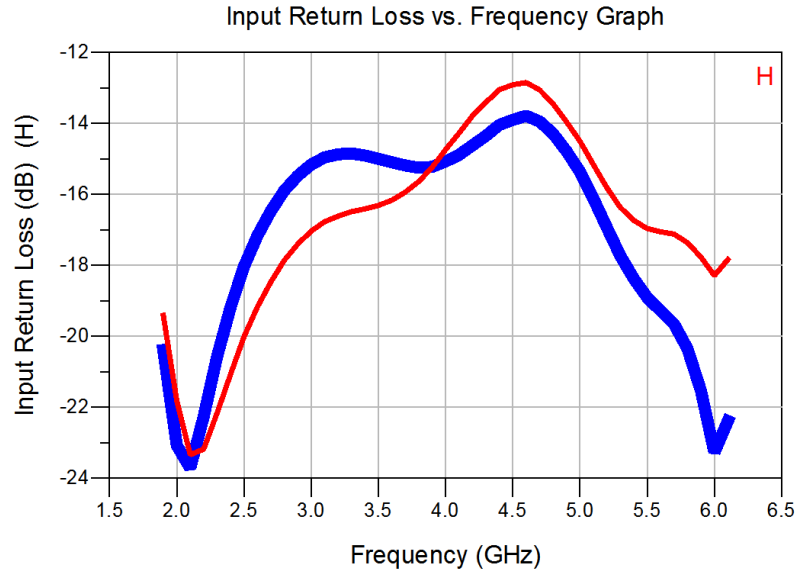


Figure 3.38. Input Return Loss EM Simulation Result (Red: Separate, Blue: Together)

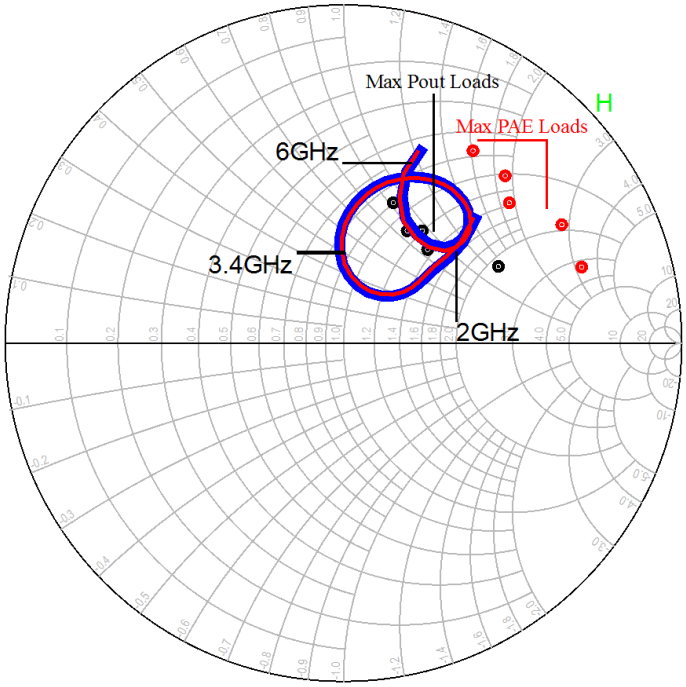


Figure 3.39. Inter-stage Matching EM Simulation Result (Red: Separate, Blue: Together)

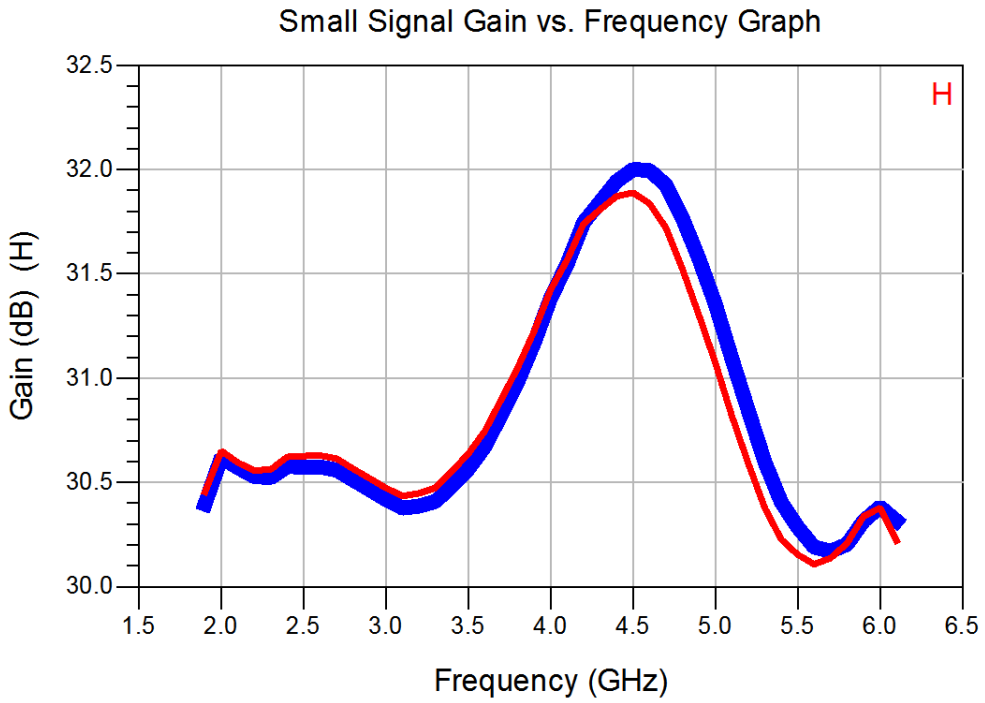


Figure 3.40. Small Signal Gain EM Simulation Result (Red: Separate, Blue: Together)

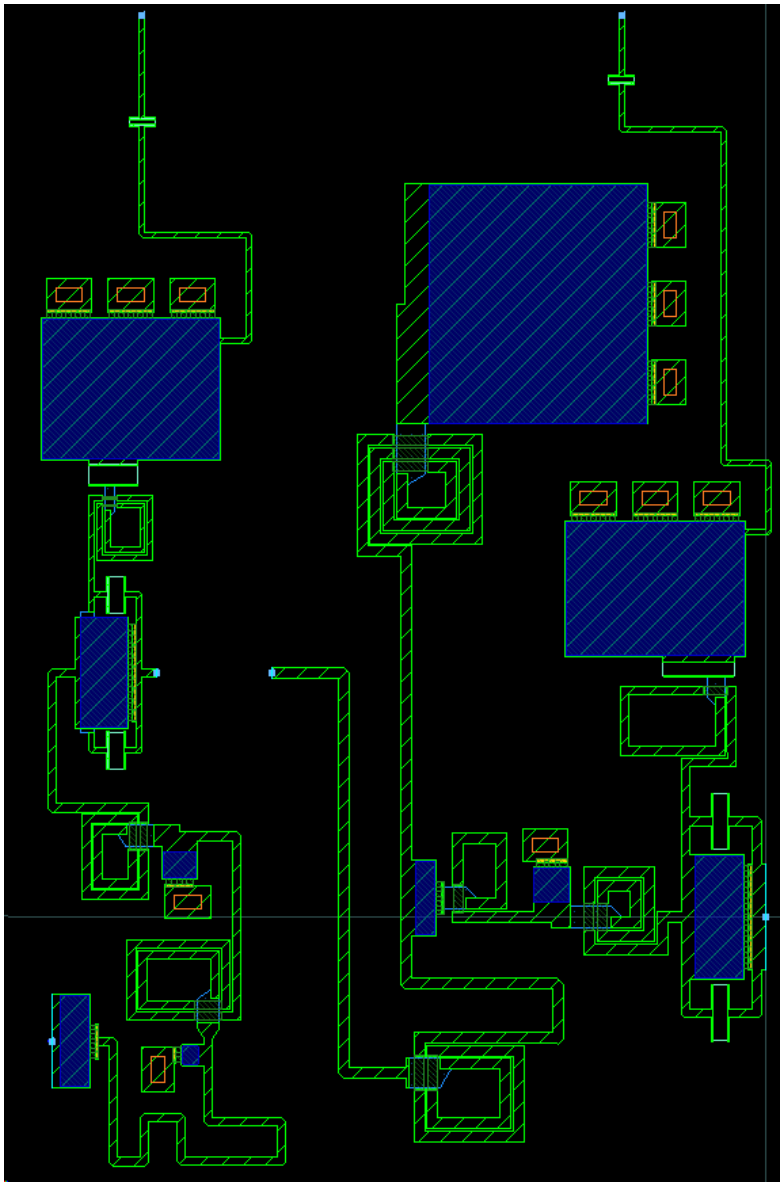


Figure 3.41. Input and Inter-Stage Matching EM Analysis Layout

Blue lines in Figure 3.38 – 3.40 are the finalized version 1 circuit results. S-Parameter measurements of the transistors are used for this circuit design. Since the PDK model is not reliable, small signal measurements are performed for 6×90 μm driver and 8×200 μm power transistors. Also, to obtain optimum loads, power and efficiency values, load-pull measurements are applied to these transistors as mentioned before. Large signal models of the transistors is not achievable for this thesis work, yet.

Therefore, large signal characteristic of the whole amplifier cannot be observed by transistor measurements. After this step, it's shown that successful small signal gain is achieved, larger than 30 dB with ±0.9 dB gain ripple. Headroom is larger than 5 dB and this means that driver transistor can drive the output power transistor without compression problem. Also, the input return loss is lower than -14 dB which is quite well for a 3 times frequency operation band amplifier.

3.6. Circuit Design: Version-2

Since GaN on SiC process is very expensive, first-run success is important for this thesis work. Production, purchasing and delivery processes take a long time, about 6 months. Therefore, moving forward with only one version is not safe to achieve first-run success. To increase the chance of first-run success, second version of the design is performed. In this second version, the main difference is PDK large-signal transistor models are used instead of transistors S-Parameter measurement results, even though the transistors large-signal models are not reliable. As mentioned before, the amplifier is designed with S-Parameter measurement results and large-signal performance is not analyzed at version-1. This version-1 circuit is shown at Figure 3.42. Dimensions of the circuit are X: 3 mm, Y: 3 mm. The input and inter-stage matchings are kept same as version-1, while only output matching is changed in version 2 to obtain higher output power and efficiency.

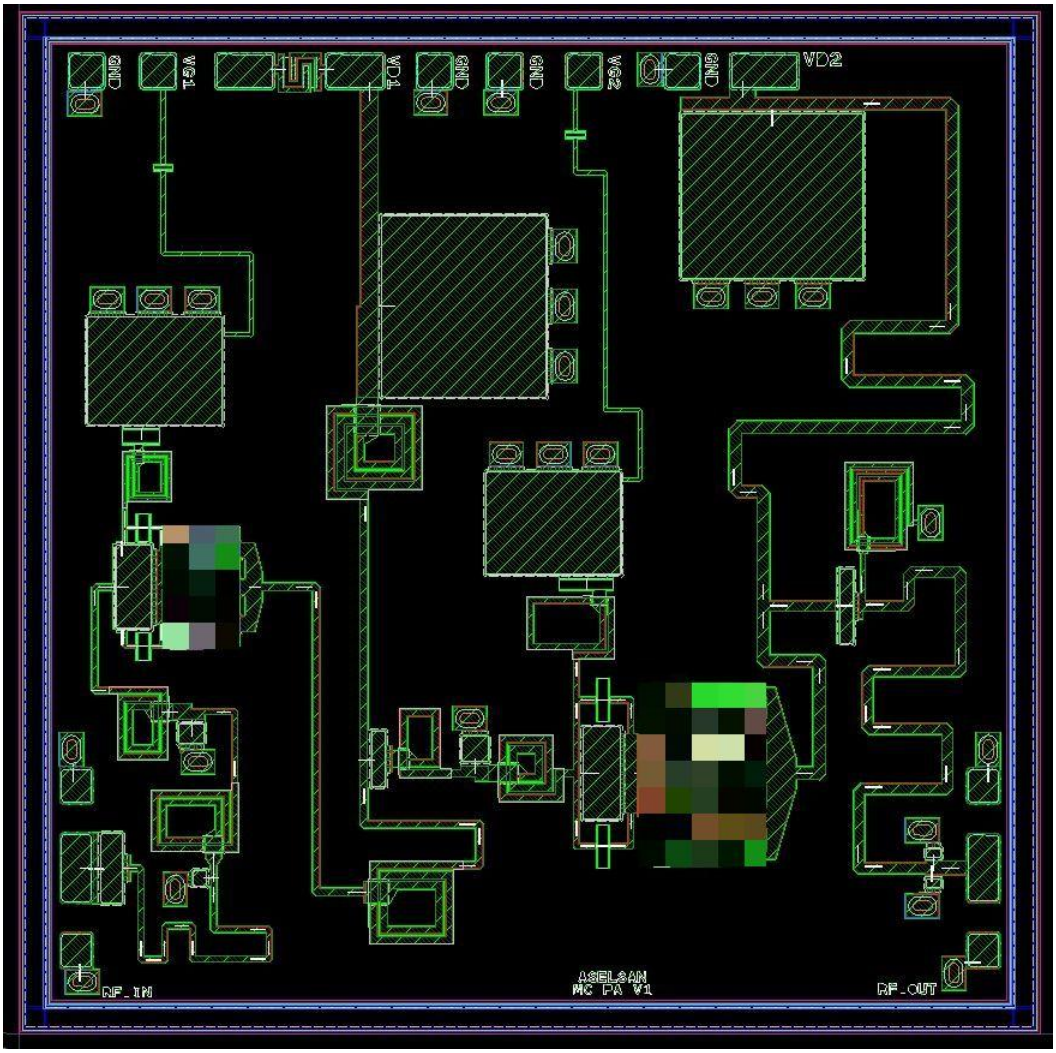


Figure 3.42. Final Layout of 2-6 GHz MMIC Amplifier Version-1 (3 mm × 3 mm)

Before starting to work with the second version, the first version is analyzed by large-signal transistor models without changing any matching circuit. Small signal gain, inter-stage impedance, output impedance and return losses are simulated. Figure 3.43 shows the small signal gain difference between transistors S-Parameter (version-1, red) and transistors large signal model (blue) simulations. As seen from Figure 3.43, there are significant differences between these two simulations. Simulations are performed at 1.9-6.1 GHz interval with 100 MHz steps.

The output matching result is observed as shown at Figure 3.44. Since PDK model doesn't affect the output matching response, the result is same as version-1. The inter-stage matching is simulated by same as small signal gain analysis. As seen from Figure 3.45, there is a small change for inter-stage matching. The mid-band is slightly away from optimum load points. This small change can be acceptable for inter-stage because of high gain of transistors.

Output and input return losses are also investigated by same way. Large-signal transistor model simulation results (blue) are slightly lower than version-1 results (red) like other performances as shown at Figure 3.46 and 3.47. These results are also acceptable for this amplifier.

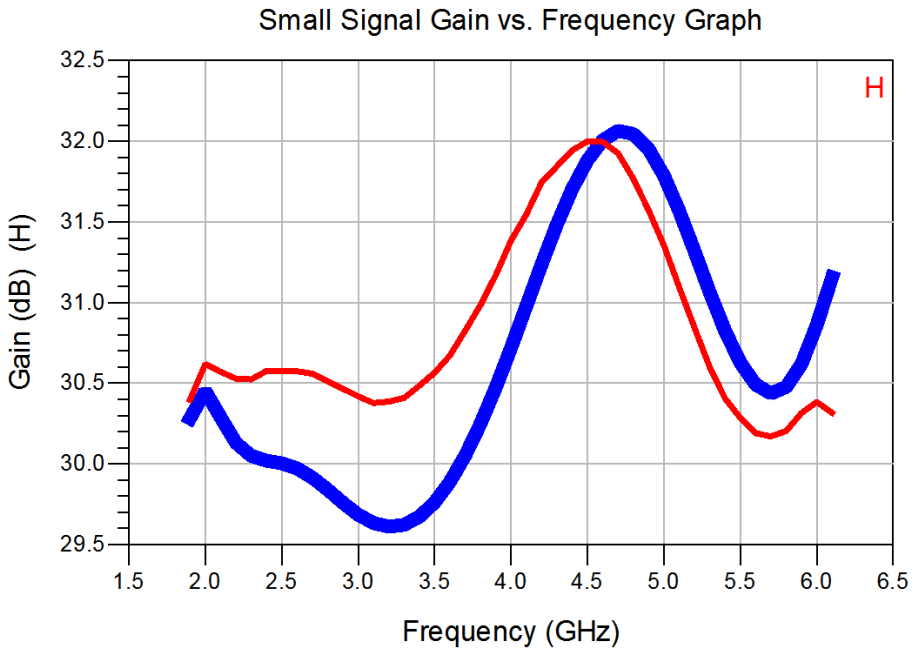


Figure 3.43. Small Signal Gain with Transistor S-Parameters (red) and PDK models (blue)

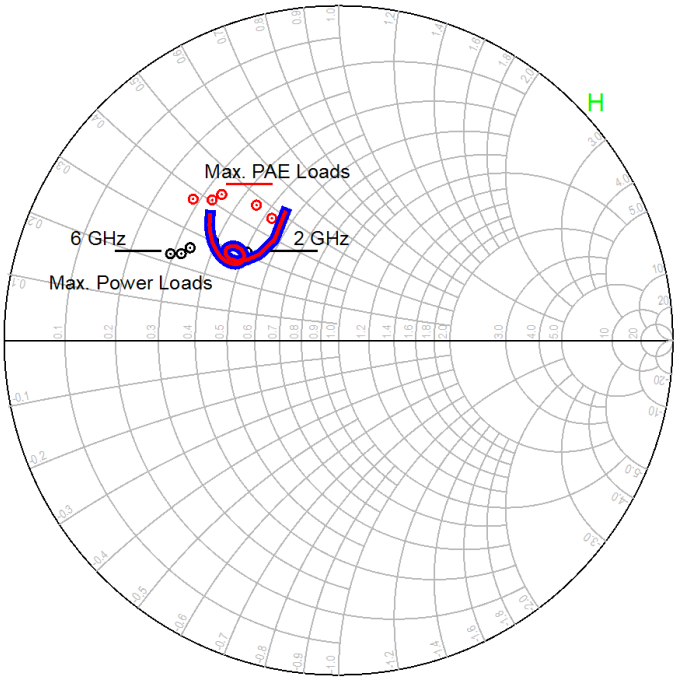


Figure 3.44. Output Matching with Transistor S-Parameters (red) and PDK models (blue)

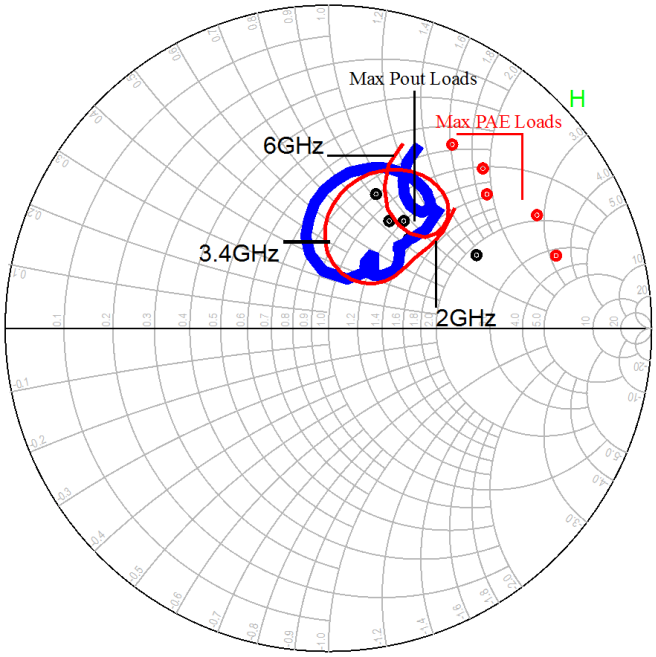


Figure 3.45. Inter-Stage Matching with Transistor S-Parameters (red) and PDK models (blue)

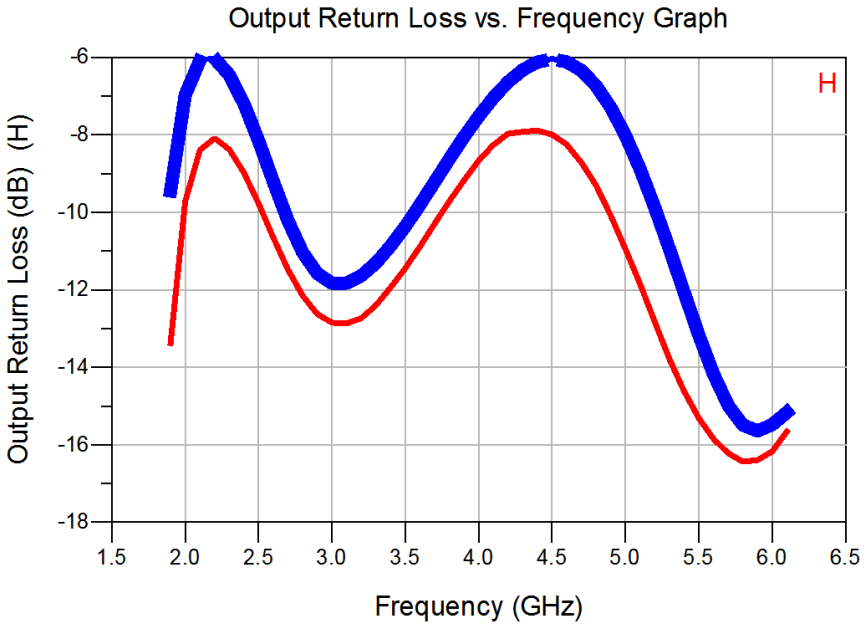


Figure 3.46. Output Return Loss with Transistor S-Parameters (red) and PDK models (blue)

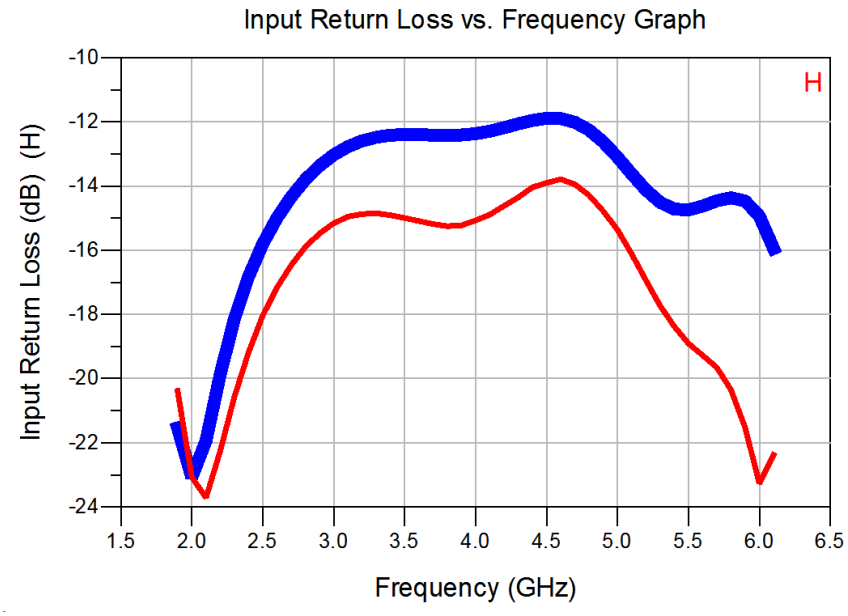


Figure 3.47. Input Return Loss with Transistor S-Parameters (red) and PDK models (blue)

The main effort of the second version is to increase output power and efficiency. The output power vs. frequency at saturation is shown in Figure 3.48. There is 1 dB power drop at around 3.2 GHz as seen in the graph. At this drop region the output power approaches to 5 W target and this increases the risk of first-run success. Also, power added efficiency (PAE) is observed with large signal PDK models. PAE result of the first version with models is shown at Figure 3.49. As seen from Figure 3.49, not only output power, but also PAE is getting lower at around 3.2 GHz. Therefore, the aim for the second version is to increase output power and PAE at 3.2 GHz and make the design safer.

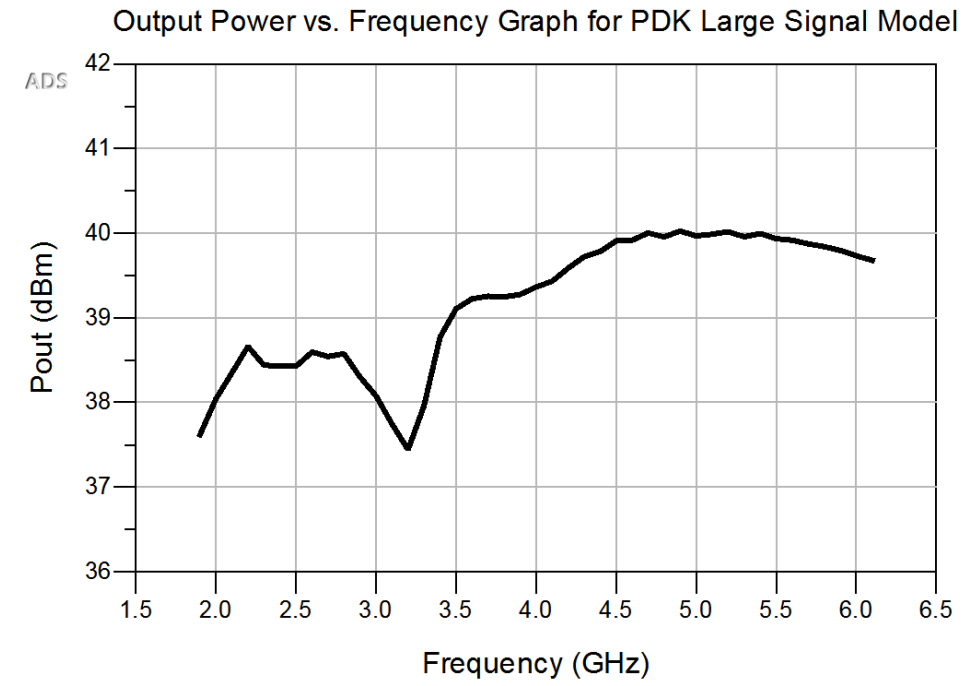


Figure 3.48. Output Power vs. Frequency Graph for PDK Large Signal Model

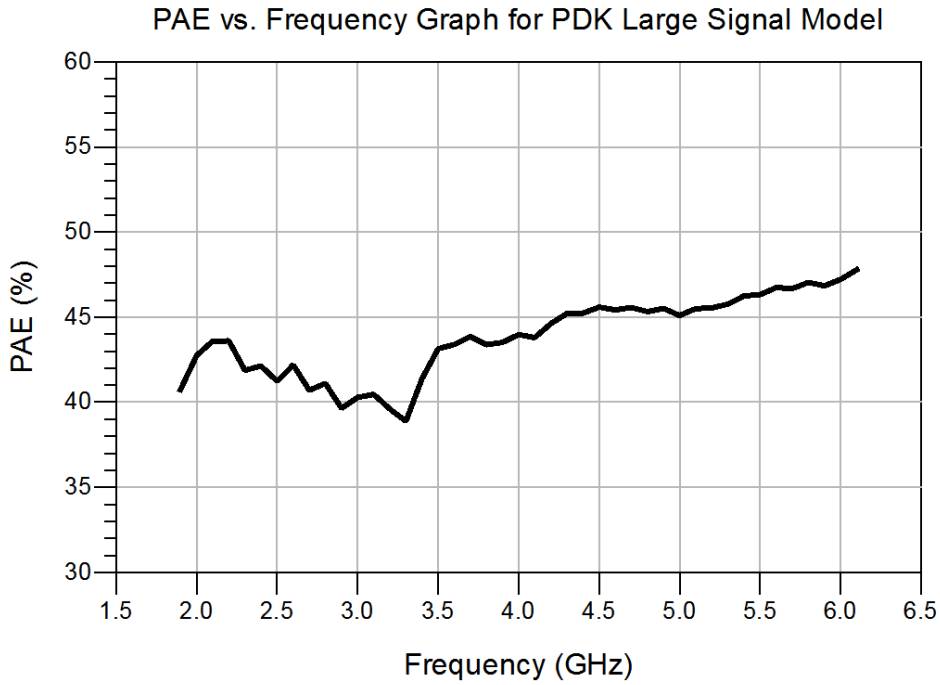
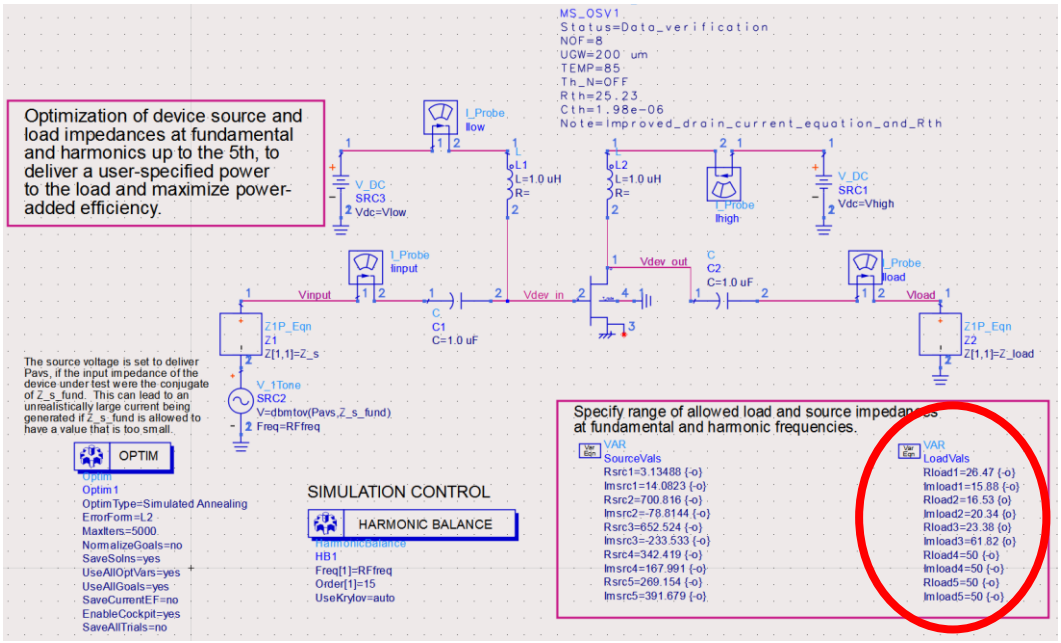


Figure 3.49. PAE vs. Frequency Graph for PDK Large Signal Model

To achieve the second version goal, simulations were performed for each of the matching circuits. It was observed that the output matching is more effective for this power drop at 3.2 GHz. During these output matching analysis, 6.4 GHz and 9.6 GHz matching improves the 3.2 GHz power and efficiency. The reason for this is the harmonics effect of the 3.2 GHz. When second and third harmonic matching points change, it effects around 3.2 GHz RF characteristics. Figure 3.50 shows an example of transistor harmonic load simulation which shows harmonic loads effect on power and efficiency. At this harmonic load simulation, fundamental load is kept constant as 26.47 + j×15.88 Ω (which is 3.2 GHz output matching load of version-1) while second and third harmonic loads are moved from version-1 output matching values to observe output power and PAE. The red circle on the Figure 3.50 shows the load variables part and bottom part of the figure shows the result. The change of harmonic loads increase the output power almost 0.5 dB and PAE 7.5%. From this analysis it can be said that harmonics should be considered during design of broadband amplifiers which harmonics included in fundamental operation frequencies.

Unfortunately, this harmonics effects can be tuned limitedly. For example, 2 GHz second and third harmonic (4 GHz and 6 GHz) is in the fundamental operation frequency and all matchings should be performed to obtain maximum performances at 4 GHz and 6 GHz as well. Therefore for this thesis work, the main focus of output matching tuning is at 3.2 GHz. However, a disadvantage for this is the 6 GHz RF performances. The tuning should be performed at the acceptable expense of the 6 GHz performance drop.

Considering all these fundamental and harmonics concepts, output matching was tuned to increase power and efficiency by using PDK large-signal model. After schematic tuning process is done, EM simulation for output matching is carried out in similar way with version-1. Obtained power and efficiency responses after this version-2 output matching simulations are shown at Figure 3.51 and Figure 3.52, respectively. As seen from the Figure 3.51, output power at 3.2 GHz is increased almost 1 dB. Output power is higher than 38 dBm (6.3 W) at whole 2-6 GHz operation band. Since unexpected effects may be occurred, this power level is much safer than version-1. PAE is also enhanced 5% at 3.2 GHz, while it decreases at 6 GHz. Another critical point here is that high output power and efficiency are expected generally at low band of the amplifier. Since antenna gain in systems is higher at higher frequencies, 6 GHz power and efficiency drop in this version-2 can be acceptable. 3.2 GHz power and efficiency raise is much critical in this microwave system perspective. As a result, version-2 updated PAE is higher than 40% at all frequency operation band and much safe than version-1 by considering 40% PAE target.



Power-Added Efficiency, %	Power Delivered to Load, dBm	Watts
59.186	39.523	8.960
66.749	40.010	10.024

Figure 3.50. Harmonic Load Simulation Schematic and Result

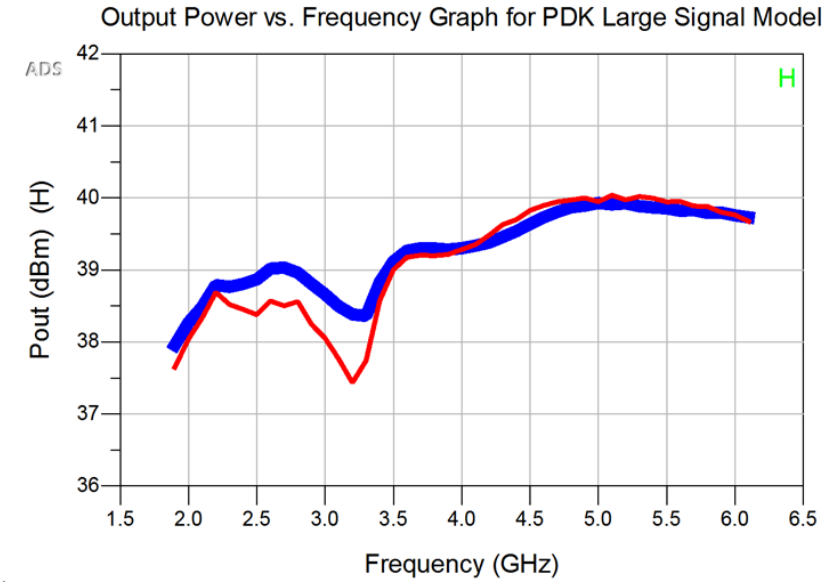


Figure 3.51. Output Power vs. Frequency Graph of Version-2 with PDK Large Signal Model (Blue: Version-2, Red: Version-1)

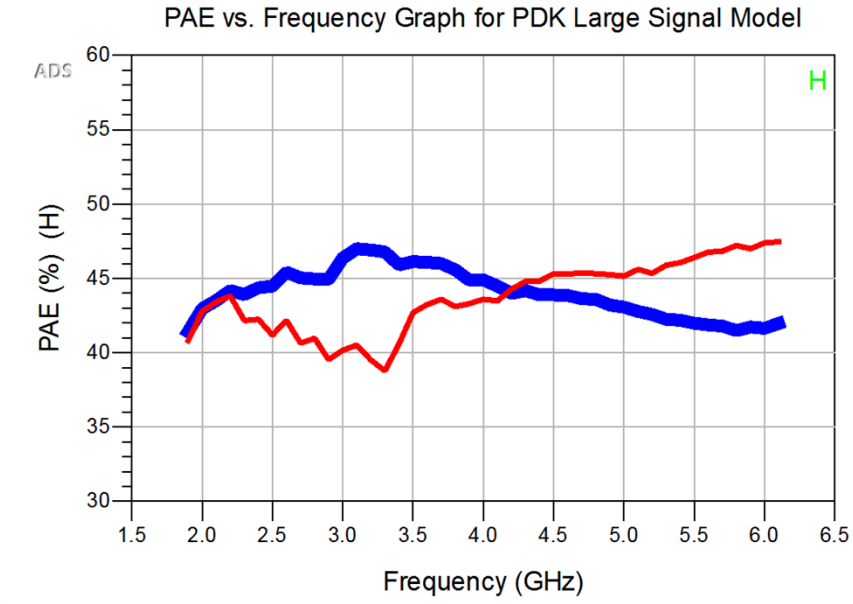


Figure 3.52. PAE vs. Frequency Graph of Version-2 with PDK Large Signal Model (Blue: Version-2, Red: Version-1)

Since the output matching circuit is changed, final output load situation should be examined at fundamental operation frequencies. The output impedance is diverged from the optimum target loads at the upper band (5-6 GHz) as seen in Figure 3.53. Here the simulation is performed from 1.9 GHz to 9.6 GHz to cover harmonics as well. Blue line is for version-2 while red one is for version-1. Unfortunately, this creates a risk to achieve maximum power and efficiency from transistors. This can be considered as a disadvantage of the version-2 as mentioned before, but almost same output power is observed at this upper band with respect to PDK models as seen in Figure 3.51. Also, the thesis output power target is 5 W (37 dBm) and higher than 39 dBm is obtained at the upper band. This increases the chance of this upper band output power risk. This version-2 can improve output power flatness by increasing lower-and and decreasing upper-band in limits. It will be understood that which simulation way is much effective for first-run success after measurements. Then, improvements will be done as a future work. Therefore, this risk is accepted for this new version.

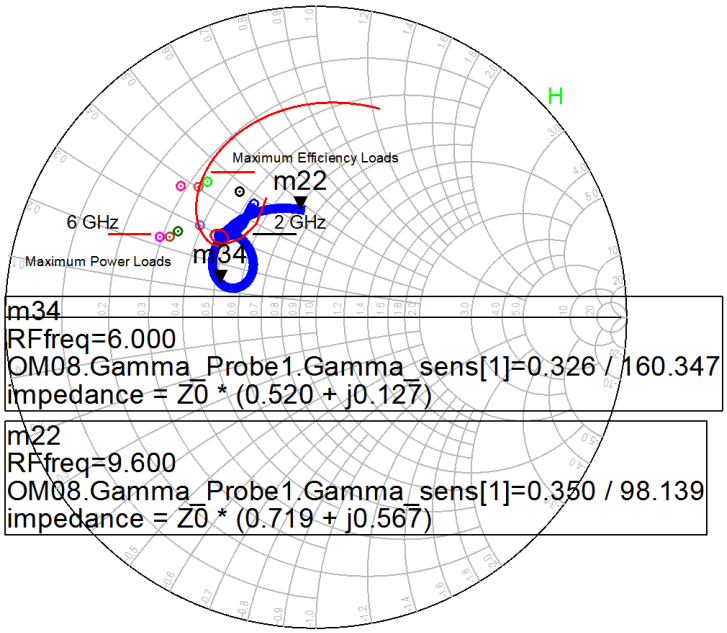


Figure 3.53. Output Matching Impedance Result (Blue: Version-2, Red: Version-1)

Output matching loss is also analyzed in this version. Lower matching loss is achieved by this new version as seen in Figure 3.54 where blue line is version-2 and red one is version-1 again. This results as higher output power (~0.2 dB) at 6 GHz and decreases the risk of lower output power because of diverged matching.

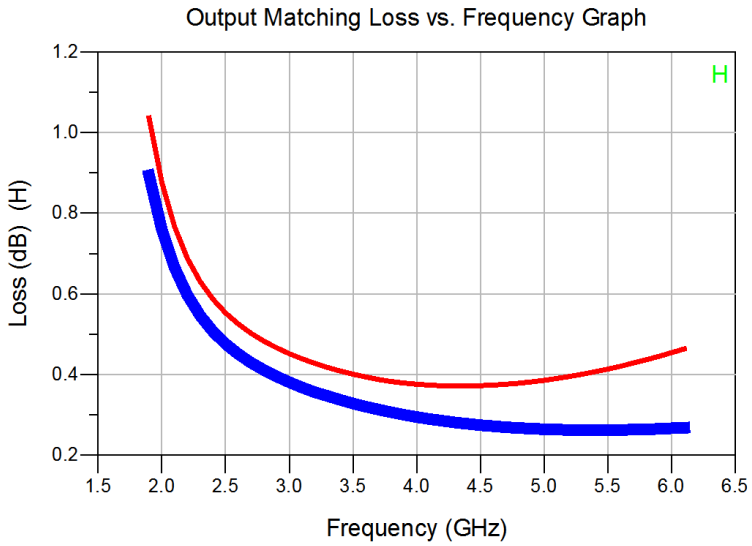


Figure 3.54. Output Matching Loss vs. Frequency Graph (Blue: Version-2, Red: Version-1)

Even small signal gain and return loss performances are unreliable since transistor layout is changed during the design, these parameters are also investigated. These results may help for the observation of the version-2 measurements. Figure 3.55 presents the small signal gain characteristic of the amplifier. Red line in Figure 3.55 shows the version-1 small signal gain with large-signal PDK models and blue line shows the version-2 final small signal gain. Gain flatness is increased in this version from ±1.25 dB to ±1 dB while larger than 29.6 dB small signal gain is achieved. Output and input return losses are showed at Figure 3.56 and Figure 3.57 respectively.

After all these analysis, final schematic view of the circuit is shown in Figure 3.58. Schematic structures of both versions are same except values of output matching components. Therefore the view is provided for both versions. Final layout of the version-2 is also shown in Figure 3.59. This circuit design is fabricated with this layout. Dimensions of the version-2 circuit is X: 2890 μm, Y: 3000 μm. Version-2 circuit x dimension is 110 μm lower than version-1 as y dimension is kept unchanged.

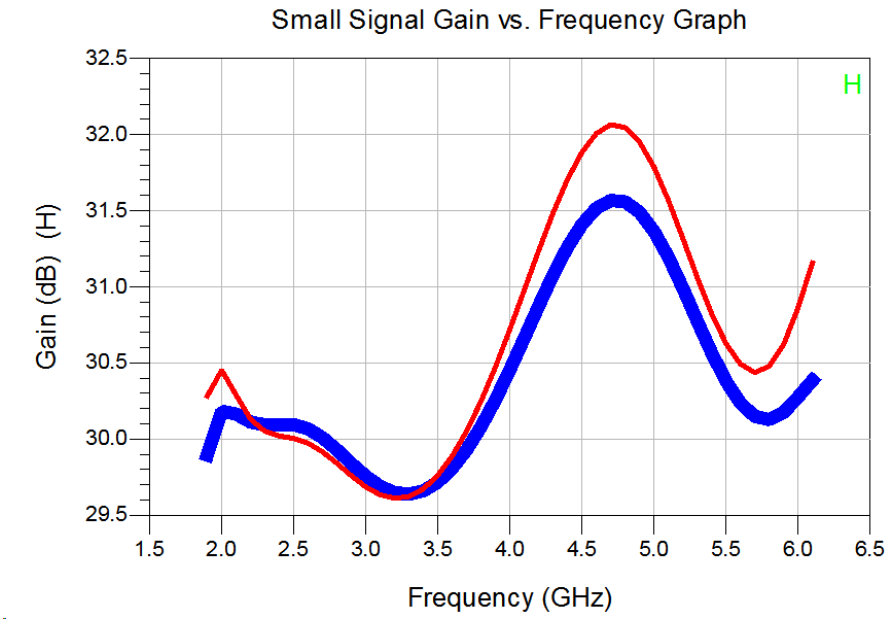


Figure 3.55. Small Signal Gain vs. Frequency Graph (Blue: Version-2, Red: Version-1)

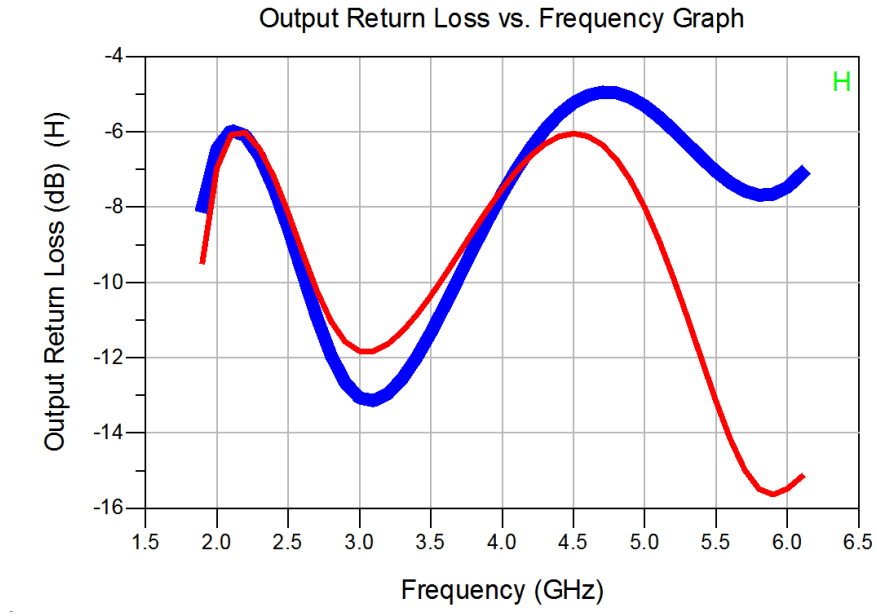


Figure 3.56. Output Return Loss vs. Frequency Graph (Blue: Version-2, Red: Version-1)

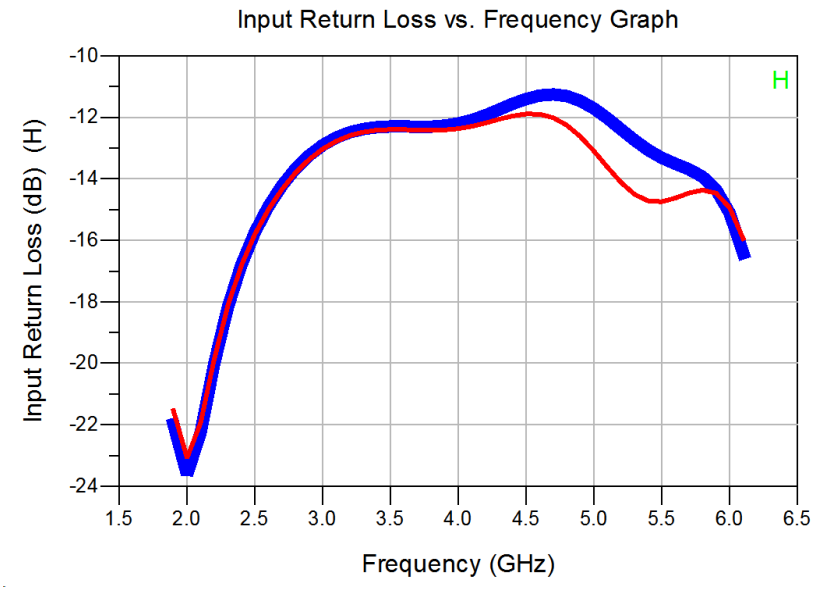


Figure 3.57. Input Return Loss vs. Frequency Graph (Blue: Version-2, Red: Version-1)

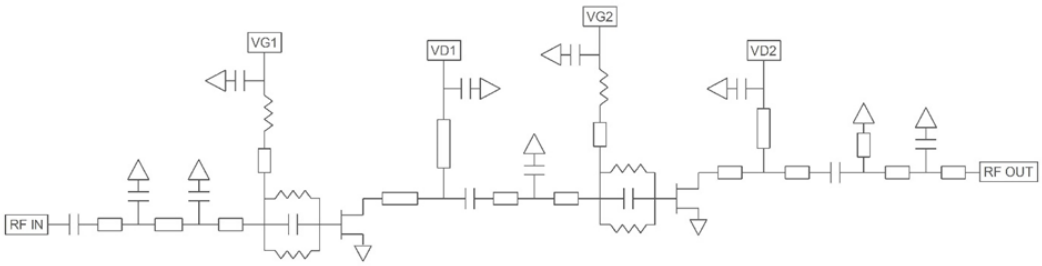


Figure 3.58. Schematic Structure of 2-6 GHz MMIC Amplifier Circuits

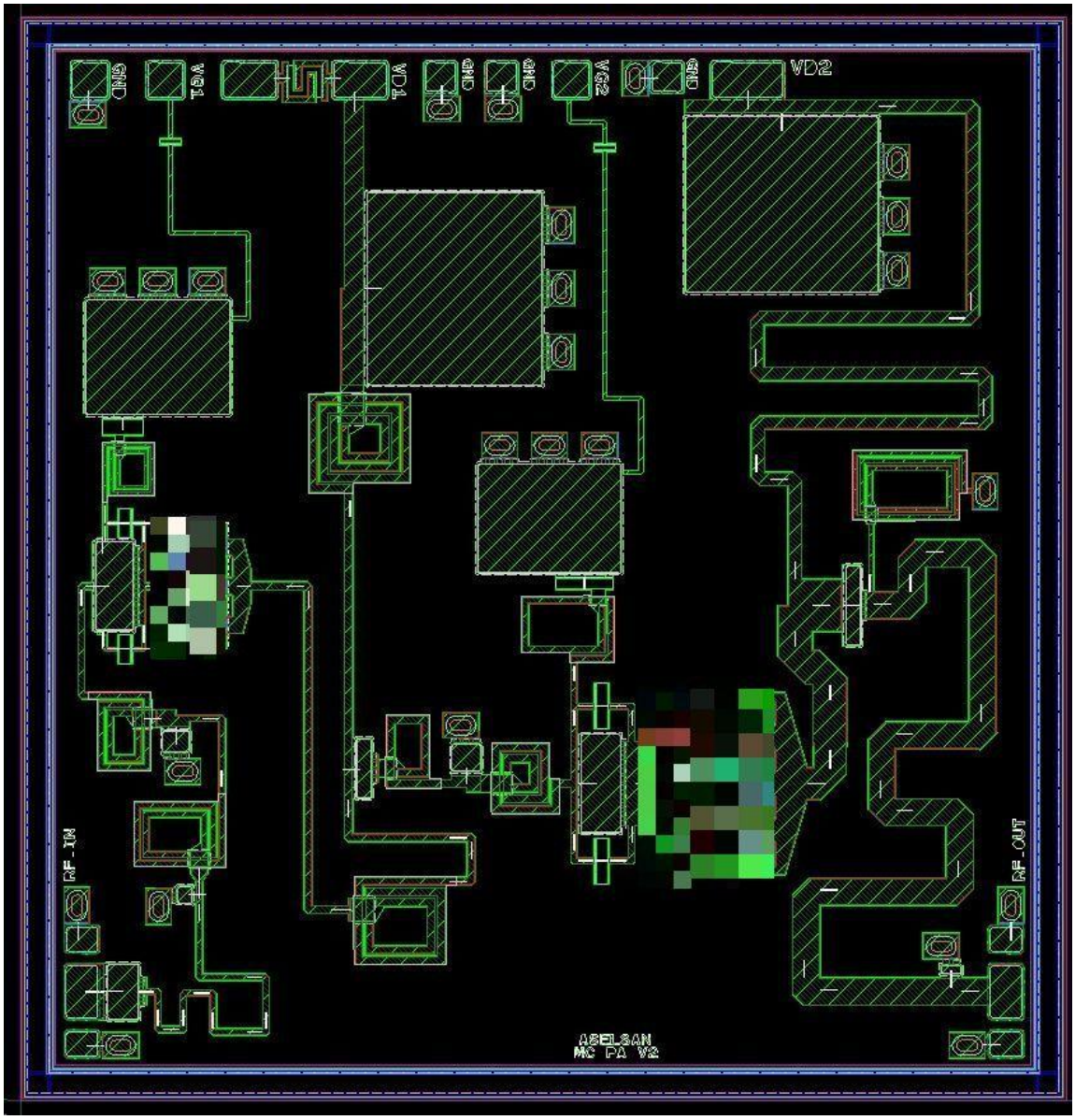


Figure 3.59. Final Layout of 2-6 GHz MMIC Amplifier Version-2
(2890 µm × 3000 µm)

CHAPTER 4

2-6 GHz GaN HEMT MMIC AMPLIFIER MEASUREMENT

Measurement of fabricated dies are final and critical part of the thesis work. All steps of measurement process should be performed carefully to obtain correct results. Devices should be checked and calibrated before measurements. Also, oscillation precautions should be prepared by off-chip capacitors and resistors before starting DC and RF tests. Moreover, power levels should be considered and sufficient attenuators should be used before power meters or network analyzers.

After around 5 months of production process, fabricated dies are received and preparations for measurements are started. Fabricated dies are shown in Figure 4.1 and Figure 4.2.

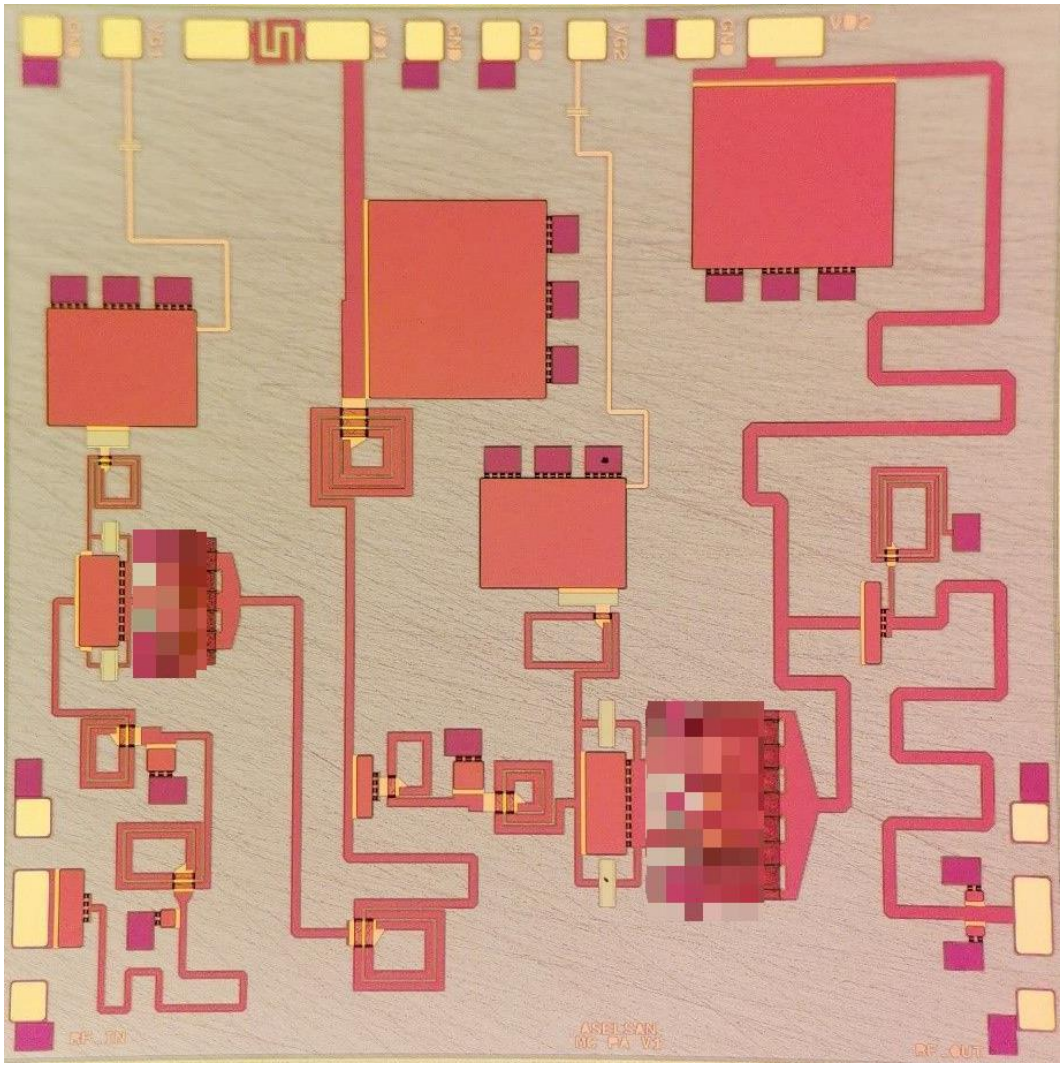


Figure 4.1. Fabricated Version-1 Die

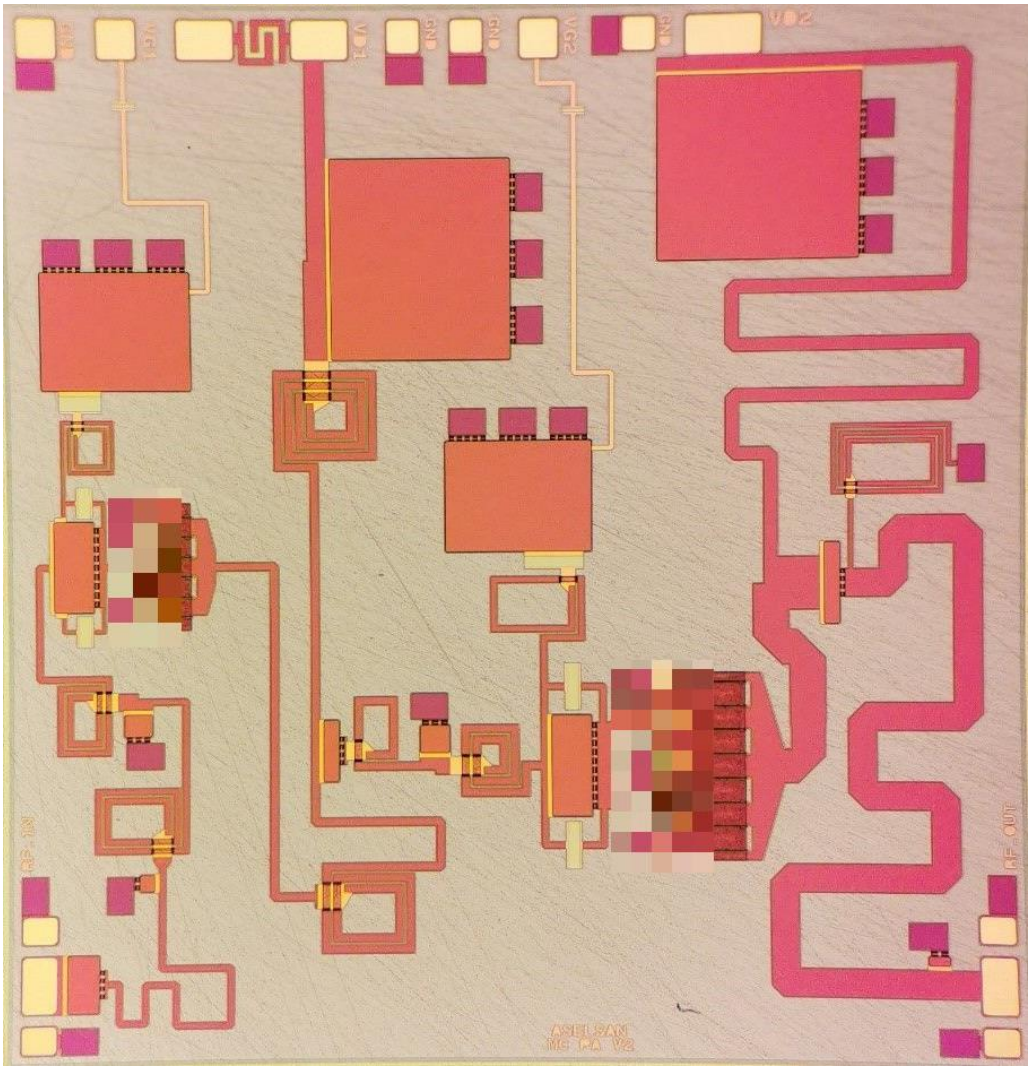


Figure 4.2. Fabricated Version-2 Die

For the measurements, MMIC dies are mounted on copper tungsten carrier with thermal epoxy. Then, 91 pF single layer capacitors are used next to gate DC pads. 10 nF single layer capacitors are also used next to drain DC pads. Not only these capacitors, but also 1 μF surface mount capacitors and 10 Ω surface mount resistors are used on both gate and drain DC bias lines as oscillation precautions. The application circuit with off-chip components is drawn as shown in Figure 4.3. Printed circuit boards are used as bias circuits. Bond wires provide the connection between DC pads of dies and PCB. After carriers for both versions are ready, on-wafer and connectorized module setups are used for measurements.

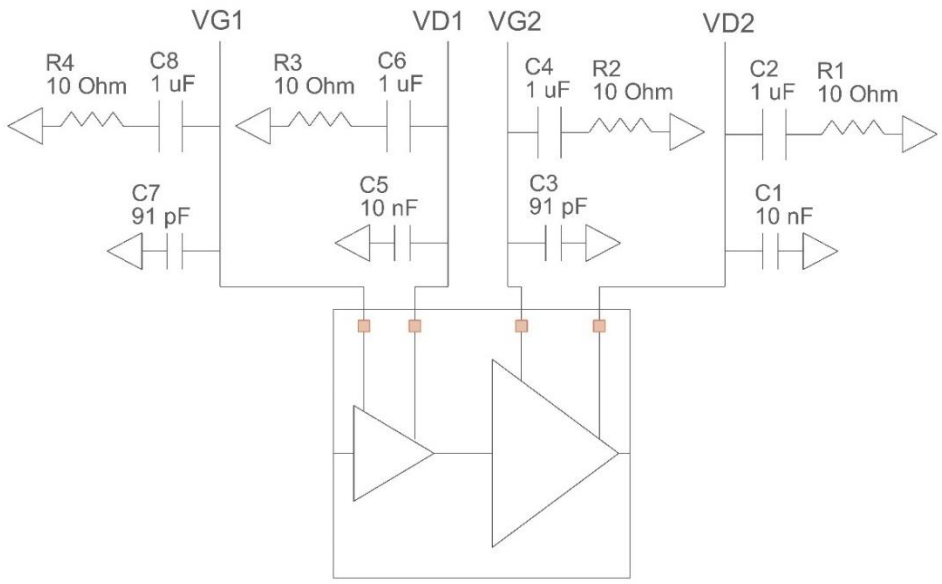


Figure 4.3. Application Circuit of 2-6 GHz Amplifier included off-chip components

4.1. On-Wafer Measurements

A probe station with 150 μm pitch distance power probes, a PNA-X network analyzer, AMCAD power supplies, Maury load tuners to show 50 Ω to dies, multimeter, couplers, Agilent DC power supplies, 2-20 GHz driver amplifier and a measurement software are used for these measurements. The setup is shown in Figure 4.4. Close view of the measurement module which includes the carrier and PCBs are shown in Figure 4.5. Oscillation precautions are provided as mentioned before in this chapter of the thesis. Off-chip capacitors, bond wires, jumpers, 150μm test point and version-1 die are showed in Figure 4.6. Test point is used because of two reasons. The first one being simulations include RF input and output bond wires and the second one being RF-IN and RF-OUT pad pitch distances are different for two versions, such as version-1 pad pitch difference is 250 μm and version-2 pad pitch difference is 150 μm. Since the whole system calibration is made by 150 μm pitch distance probe, test points are used. To measure the temperature during operation of the die, temperature sensor is mounted on bottom of the die as close as the power transistor.

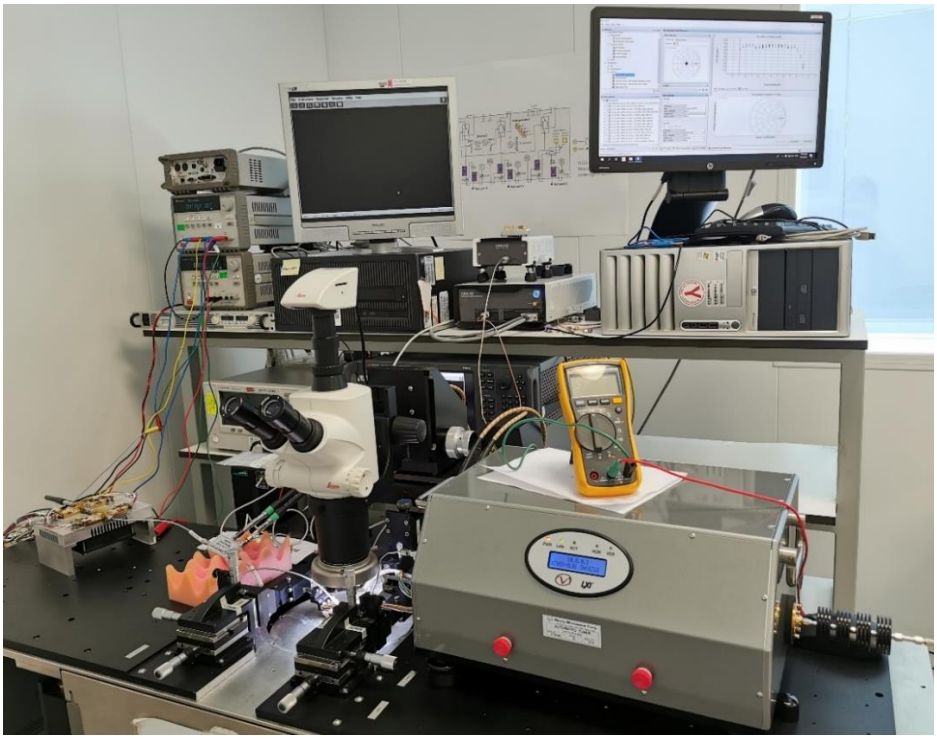


Figure 4.4. On-Wafer Probe Station Measurement Setup

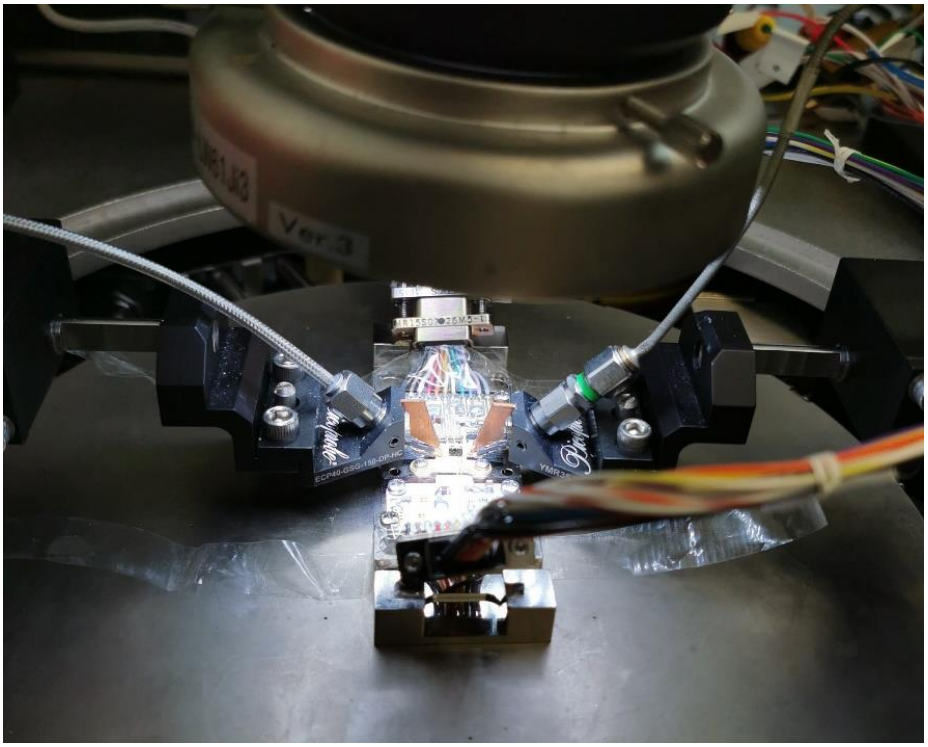


Figure 4.5. Close View of the On-Wafer Measurement Setup

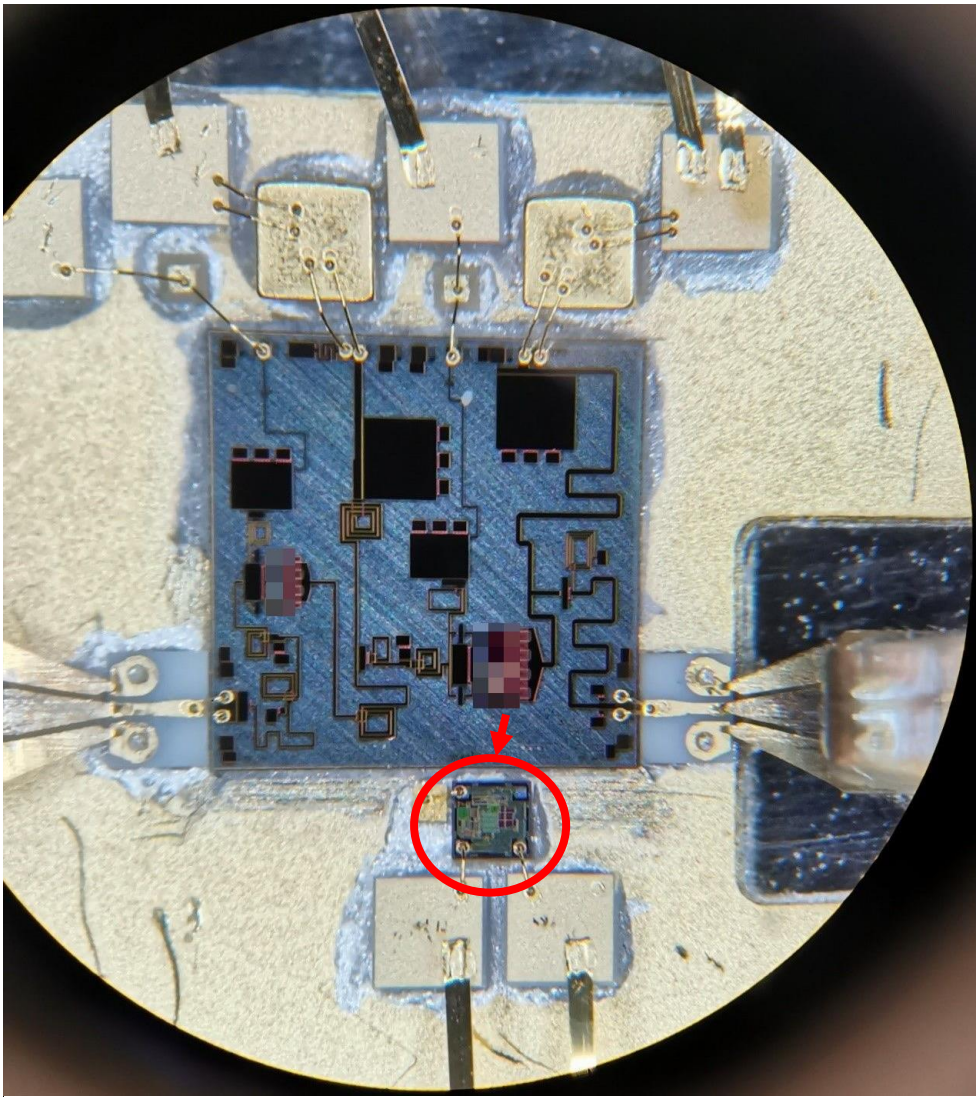


Figure 4.6. MMIC die, single layer capacitors, jumpers, test points on the carrier and probes photograph. Probes touch to 150 µm test points. Red circle shows the temperature sensor.

4.1.1. On-Wafer Large Signal Measurement Results

In this subsection, on-wafer large signal measurement results are presented. Both version measurements were performed on same setup which is shown in Figure 4.4. Results of them are also presented in same graphs to compare easily. First of all, output power and PAE results are introduced. As seen in Figure 4.7, output power characteristic at 8 dB gain compression level is similar to PDK large-signal model

simulations. Version-2 has ~0.7 dB higher output power at around 3.2 GHz and lower output power at upper band of the operation frequency as simulated before. This means that version-2 has more flat output power response as expected. The compression level can be thought high for this type of amplifier, but GaN process designs achieve maximum output levels at high compression levels, such as 5-6 dB for a stage. To show compression effect clearly, output power at 7 dB compression level is also shown at Figure 4.8. Power increment, specially at around 3.2 GHz, can be observed by these two results.

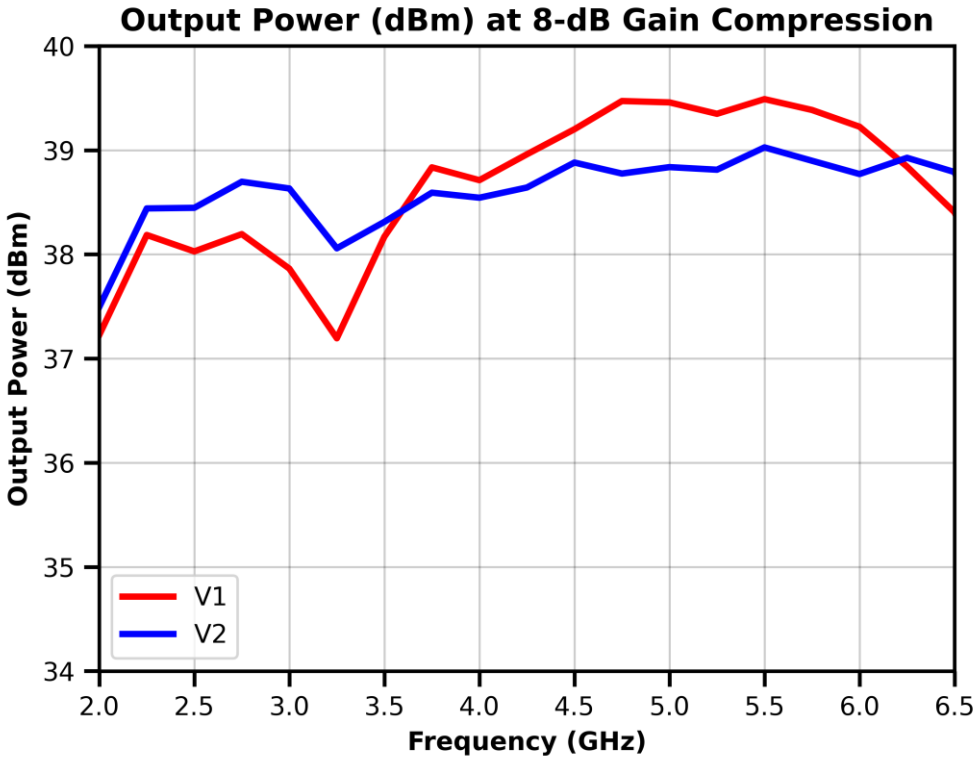


Figure 4.7. Output Power vs. Frequency Graph at 8 dB Compression

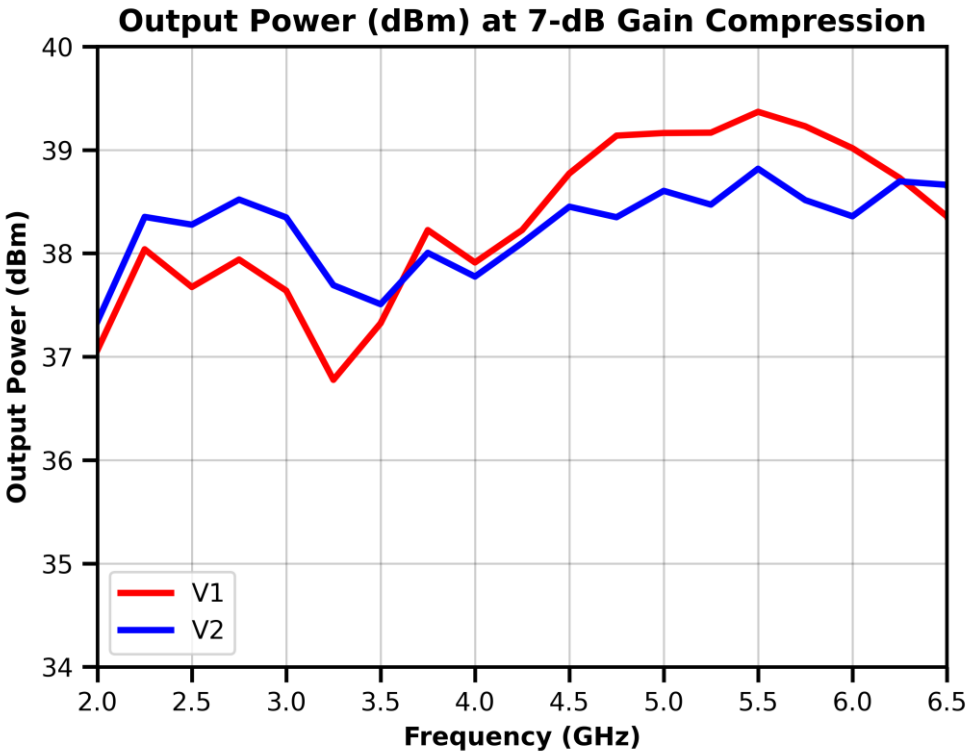


Figure 4.8. Output Power vs. Frequency Graph at 7 dB Compression

Main difference between simulations with PDK models and measurements is that the simulations have ~1 dB larger output power at upper band. PAE response of dies are shown at Figure 4.9 and Figure 4.10. Same as output power characteristics, PAE is higher at around 3.2 GHz and lower at upper-band for version-2. At upper band (4-6 GHz) PAE is 5% lower than simulations. PDK model inaccuracy at upper band may cause this difference since the model cannot take the temperature effect into account. The temperature read from the sensor is 74ºC during this analysis and input power is 16 dBm. Transistors are modeled at room temperature and simulation results don't change even at 74ºC. During measurements carrier base temperature reachs to 74ºC and this means that transistor has even higher temperature because of the position of the temperature sensor. Since PAE is lower at the upper band, the temperature effect is higher at these frequencies. This may explain why 2-4 GHz measurements are much close to simulations while 4-6 GHz aren't. The aim in these PDK model simulations was to increase 3.2 GHz response and obtain flat output

power. Therefore, the design targets are achieved for output power even at this power drop. To observe all this temperature effects, measurements could be performed at lower base temperatures. However, cooling system cannot be used efficienctly at this on-wafer probe station. Unfortunately, temperature effect cannot be observed during these on-wafer measurements.

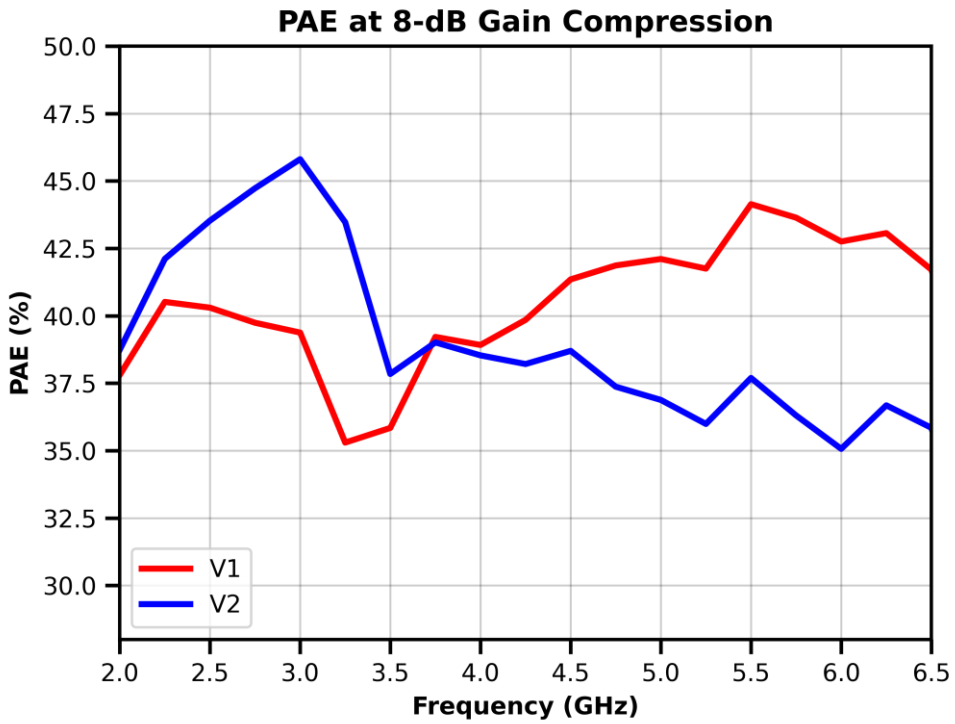


Figure 4.9. PAE vs. Frequency Graph at 8 dB Gain Compression

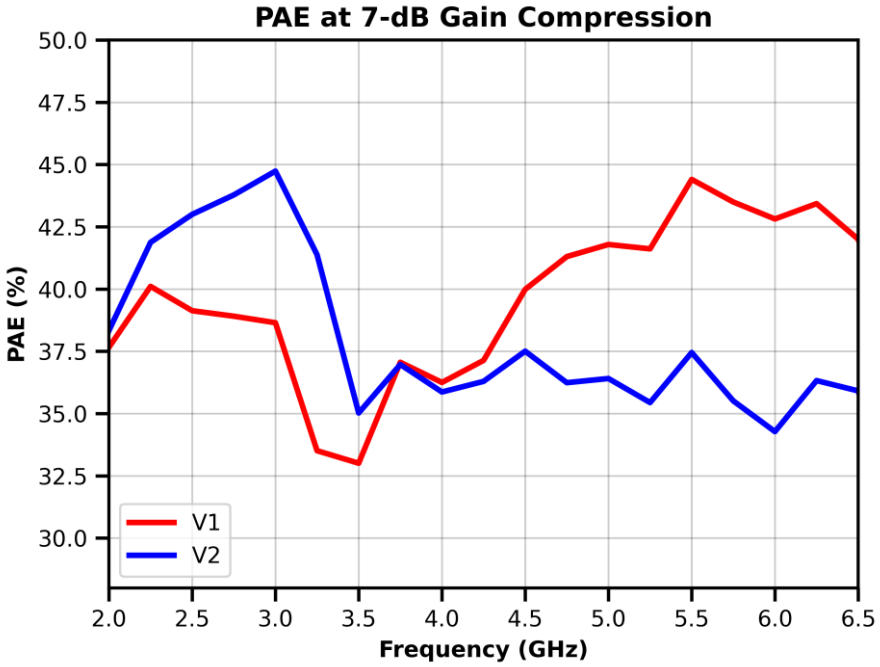


Figure 4.10. PAE vs. Frequency Graph at 7 dB Gain Compression

In gain compression analysis, input power is not constant at all frequencies in this broadband reactive matching amplifier. If the RF system cannot provide different input power levels to amplifiers, constant input power analyses are required. 8 dB gain compression level at 3.2 GHz is achieved at around 16 dBm input power. Therefore, large signal characteristics at 16 dBm input power are shown at Figures 4.11 – 4.14.

Input power sweeps are also performed during these on-wafer measurements. Figures 4.15 – 4.17 show that how input power increment affects the large signal characterictics of amplifiers. To sum up this part of on-wafer measurements, 5 W output power target is achieved at all frequency band, especially thanks to version-2 modification. Much flat gain and power response which is critical for a front-end amplifier is achieved for version-2. Achieved power and gain levels for this small die (2.89 mm × 3 mm) is successfull at this broandband operation thanks to GaN process.

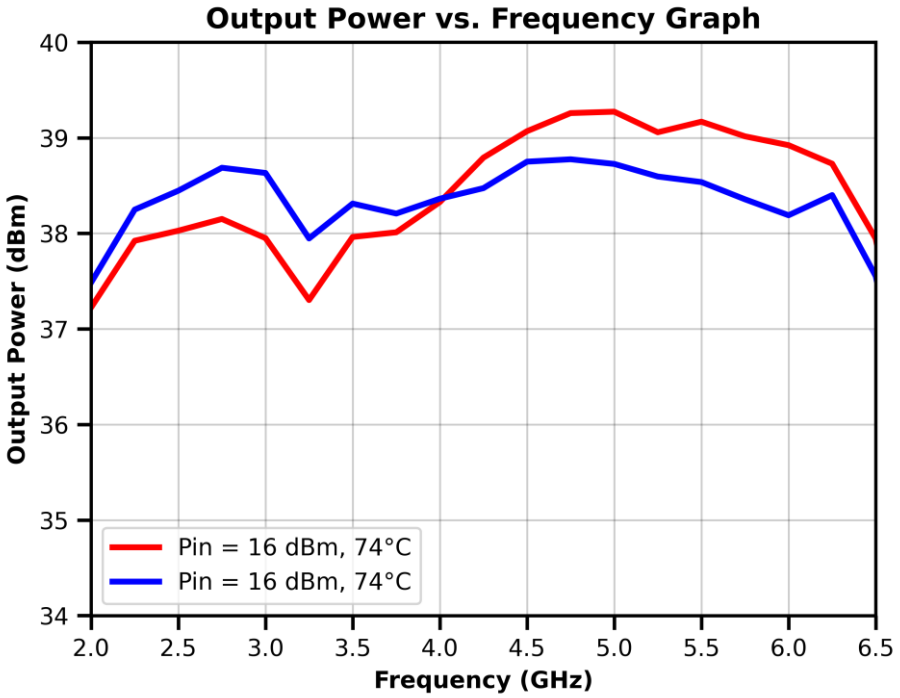


Figure 4.11. Output Power vs. Frequency Graph (Red: V1, Blue: V2)

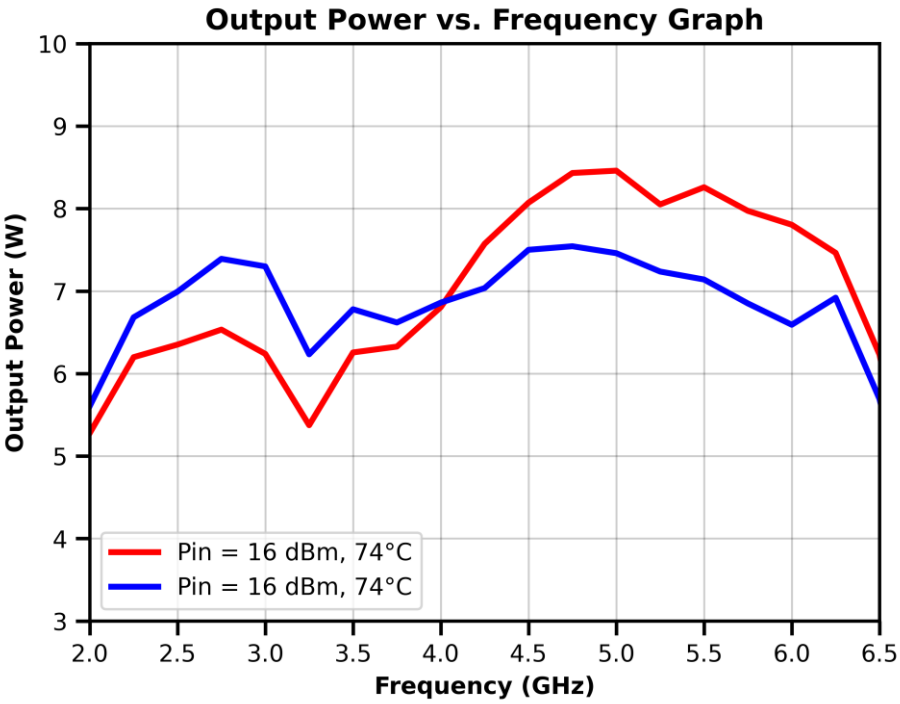


Figure 4.12. Output Power (W) vs. Frequency Graph (Red: V1, Blue: V2)

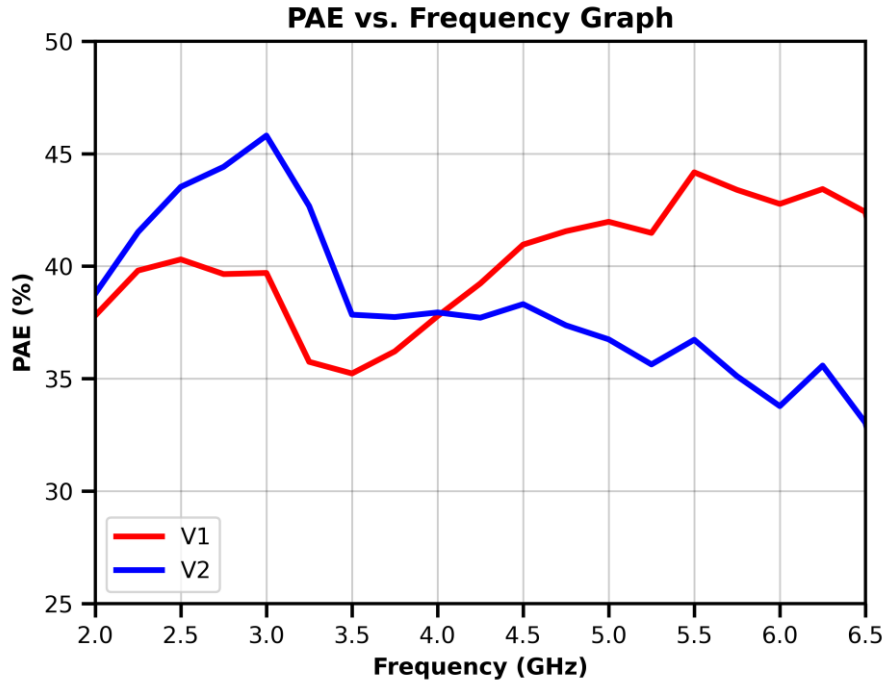


Figure 4.13. PAE vs. Frequency Graph (Pin: 16 dBm @74°C)

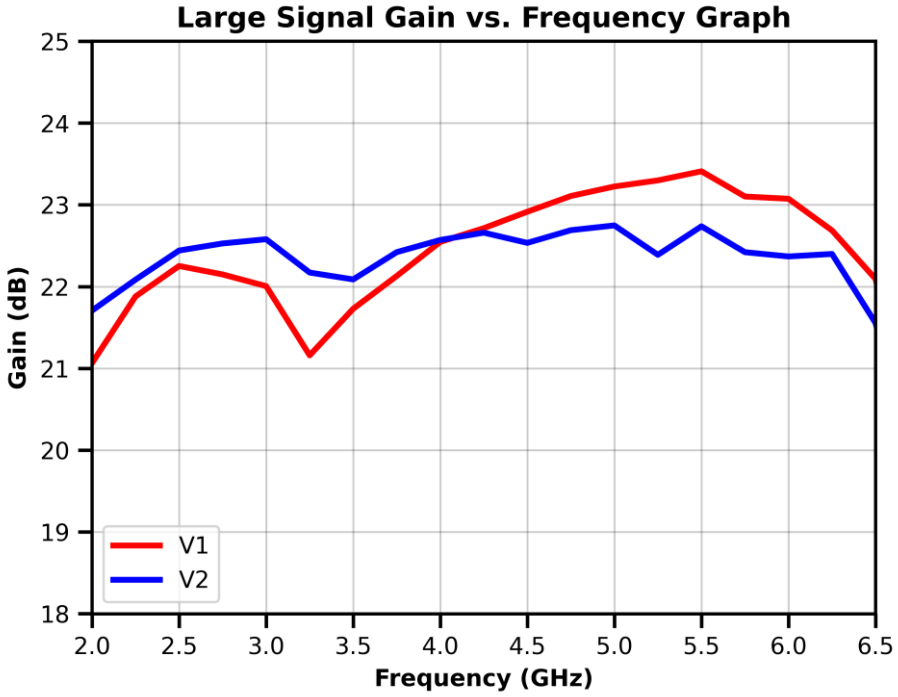


Figure 4.14. Large Signal Gain vs. Frequency Graph (Pin: 16dBm @74°C)

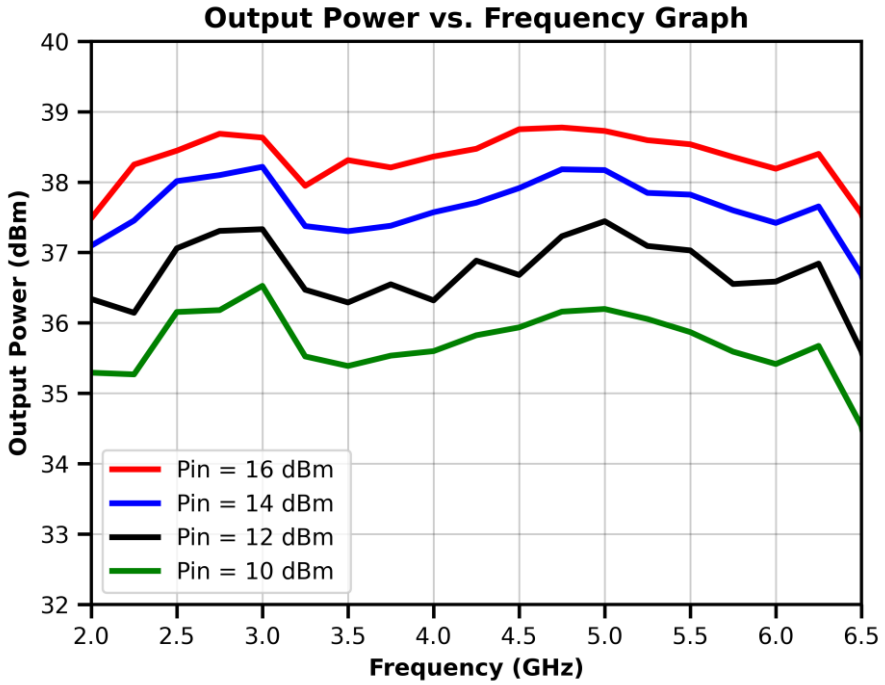


Figure 4.15. Output Power vs. Frequency Graph

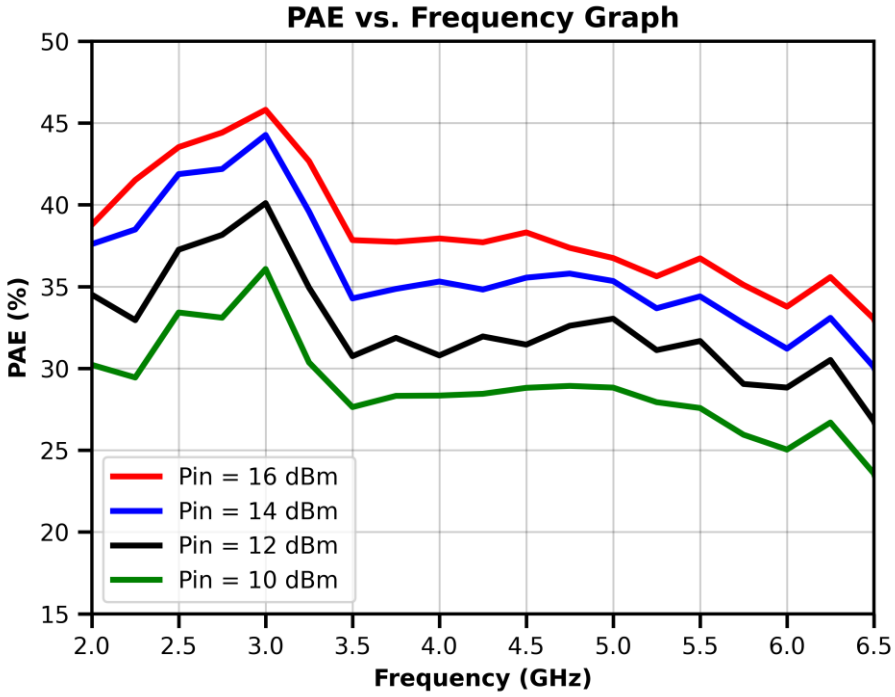


Figure 4.16. PAE vs. Frequency Graph

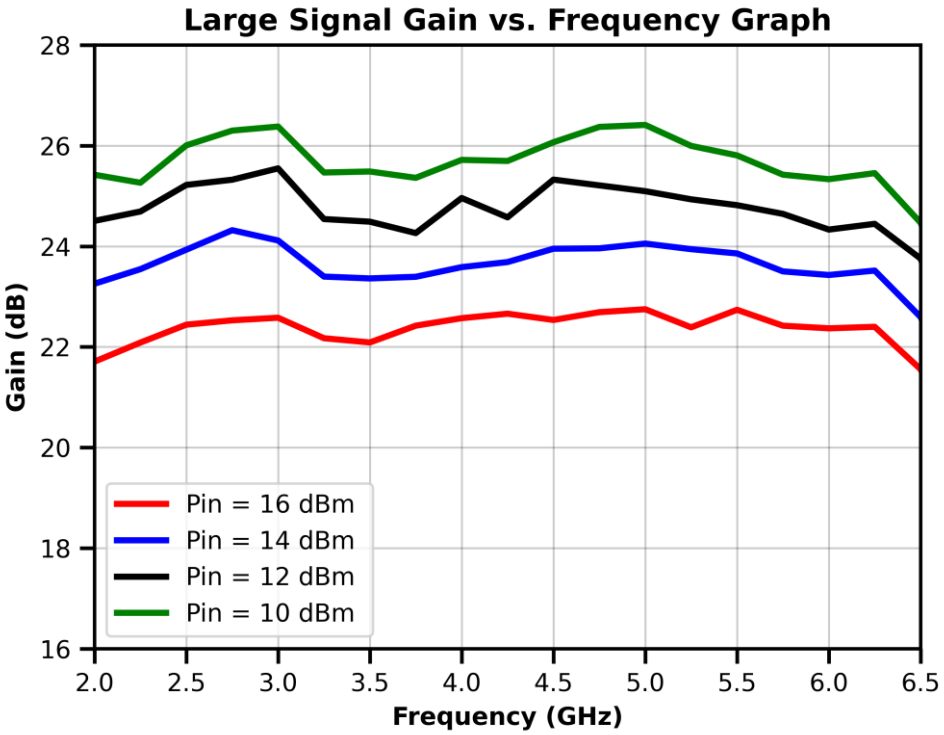


Figure 4.17. Large Signal Gain vs. Frequency Graph

4.1.2. On-Wafer Small Signal Measurement Results

Small signal characteristics of version-2 is investigated for the on-wafer setup. Small signal gain, input and output return loss measurement results are described in this subsection. For these measurements, Short-Open-Load-Thru (SOLT) calibration is performed to calibrate the system up to probe tip before die measurements. Measurement results are compared with both transistor S-Parameter and PDK model simulations. Figure 4.18 shows the small signal gain vs. frequency response of the die. Black line on Figure 4.18 represents the simulation of the amplifier with transistor S-Parameters. It can be observed that simulation results are much similar to the measurement results. In contrary to simulations with transistor S-Parameters, small signal gain response of simulation with PDK transistor models is far from the measurement results as shown in Figure 4.19. This means that it is preferrable to use transistor S-Parameters during designs to achieve successful small signal response.

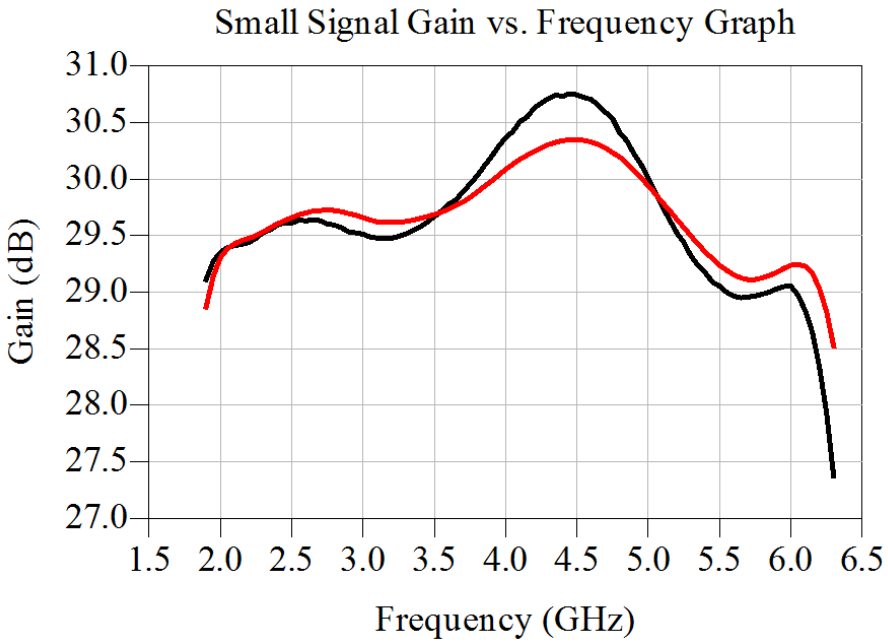


Figure 4.18. Small Signal Gain vs. Frequency Graph (Red: Measurement, Black: Simulation with transistor S-Parameter Measurements)

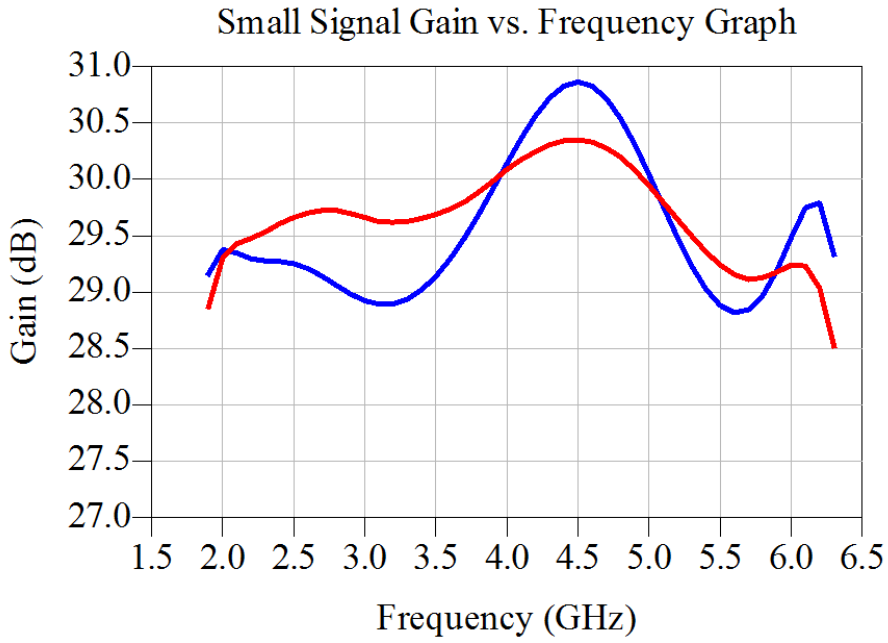


Figure 4.19. Small Signal Gain vs. Frequency Graph (Red: Measurement, Blue: Simulation with transistor PDK models)

Input and output return loss performances are also investigated in this subsection. Figure 4.20 and Figure 4.21 show output and input return loss responses respectively. Output return loss simulation is so close to measurement. However, input return loss is not close as much as output return loss.

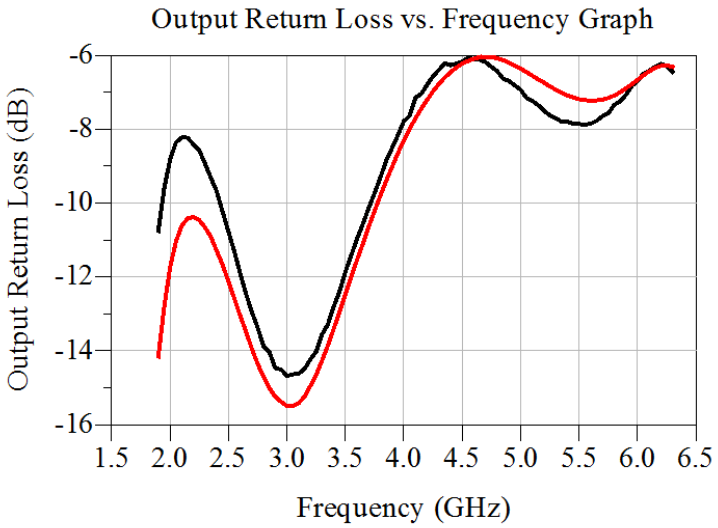


Figure 4.20. Output Return Loss vs. Frequency Graph (Red: Measurement, Black: Simulation with transistor S-Parameter Measurements)

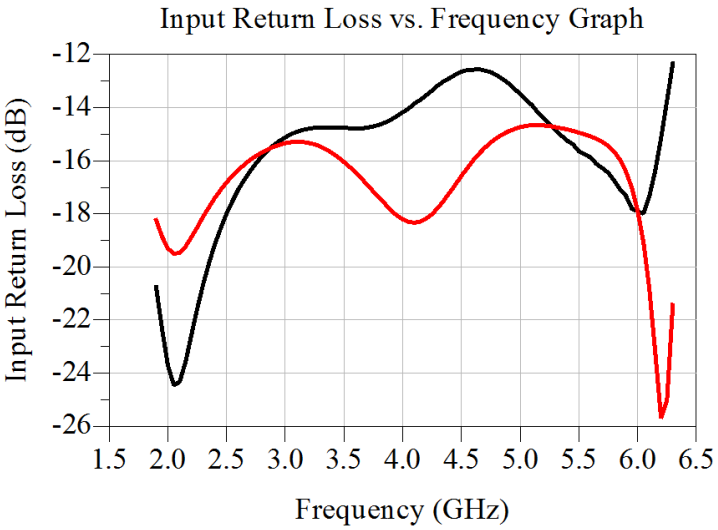


Figure 4.21. Input Return Loss vs. Frequency Graph (Red: Measurement, Black: Simulation with transistor S-Parameter Measurements)

4.2. Connectorized Module Measurements

Temperature cannot be controlled effectively at on wafer measurement setup especially when lower temperatures are essential. Therefore, another test setup is used for temperature controlled measurements as shown in Figure 4.22. This test setup includes temperature controller which can be used even at -40ºC by the help of liquid nitrogen. Version-2 die carrier is mounted on connectorized module and the module is put on the temperature controller with thermal pad between the controller and the module. This whole setup include signal generator, DC power supplies, DC to 18 GHz 25 W 40 dB attenuator, power sensor, RF cables, temperature controller and multimeter to check temperature sensor output voltage.

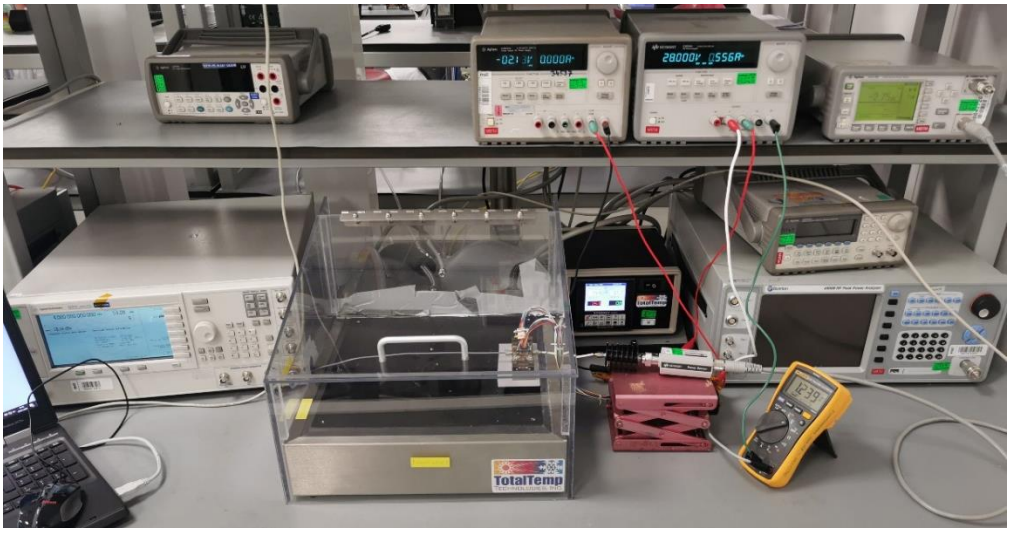


Figure 4.22. Connectorized Module Test Setup with Temperature Controller

Cables, signal generator, power sensor and attenuator are calibrated to determine power levels at input and output of the module connectors before measurements. Temperature controller is also calibrated to check its functionality. After all components of the test setup is ready, the module is measured at different temperatures. The LM20 temperature sensor is mounted next to the die on carrier as

mentioned before. Temperatures read from this sensor by the multimeter are recorded during measurements. To obtain specific temperatures, like room temperature and 85ºC, at this sensor, the temperature controller is used. For example, 22ºC carrier base temperature is obtained when the temperature controller is at -15ºC for output power and PAE measurements at 16 dBm input power.

Output power response at three different temperatures is shown in Figure 4.23. At 22ºC, almost room temperature, the output power response is almost same with the version-2 large signal simulations. Output power reach to 40 dBm at upper band like simulations. This means that PDK model transistor simulations are so close to real responses. Output power drop is observed while temperature rises as expected. PAE measurement results are also shown at Figure 4.24. It is observed that large signal simulation PAE result is close to measurement as same as output power. At 22ºC temperature, over 40% PAE is obtained at all operation band like simulated. Finally, small signal gain measurement result is provided in Figure 4.25.

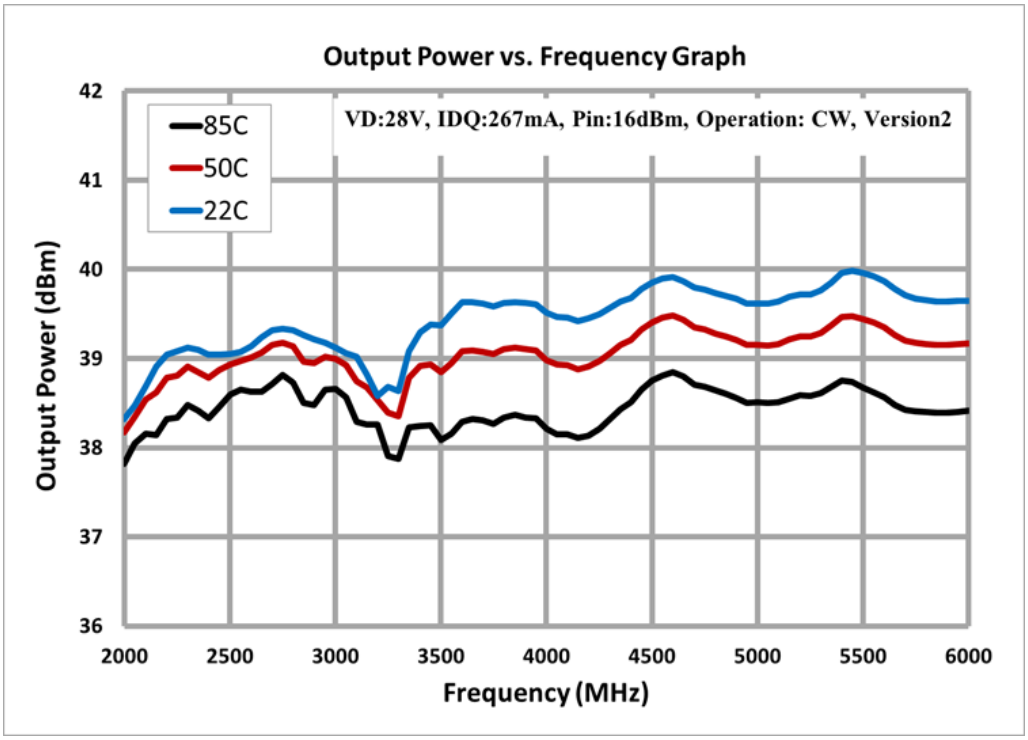


Figure 4.23. Output Power vs. Frequency Graph vs. Temperature

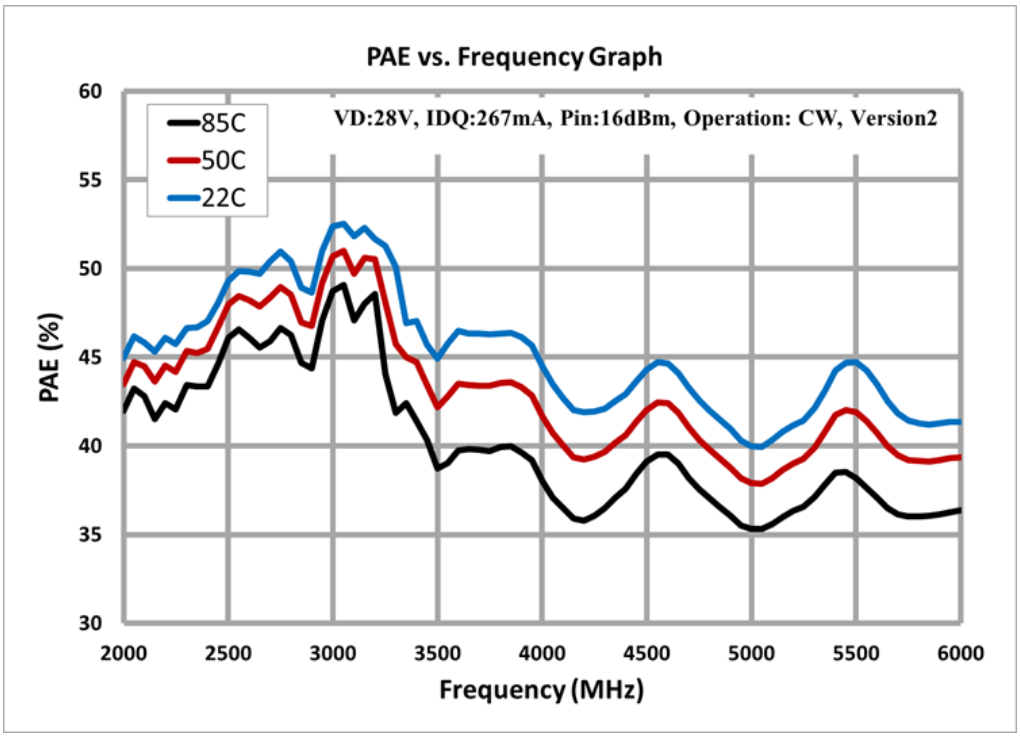


Figure 4.24. PAE vs. Frequency Graph vs. Temperature

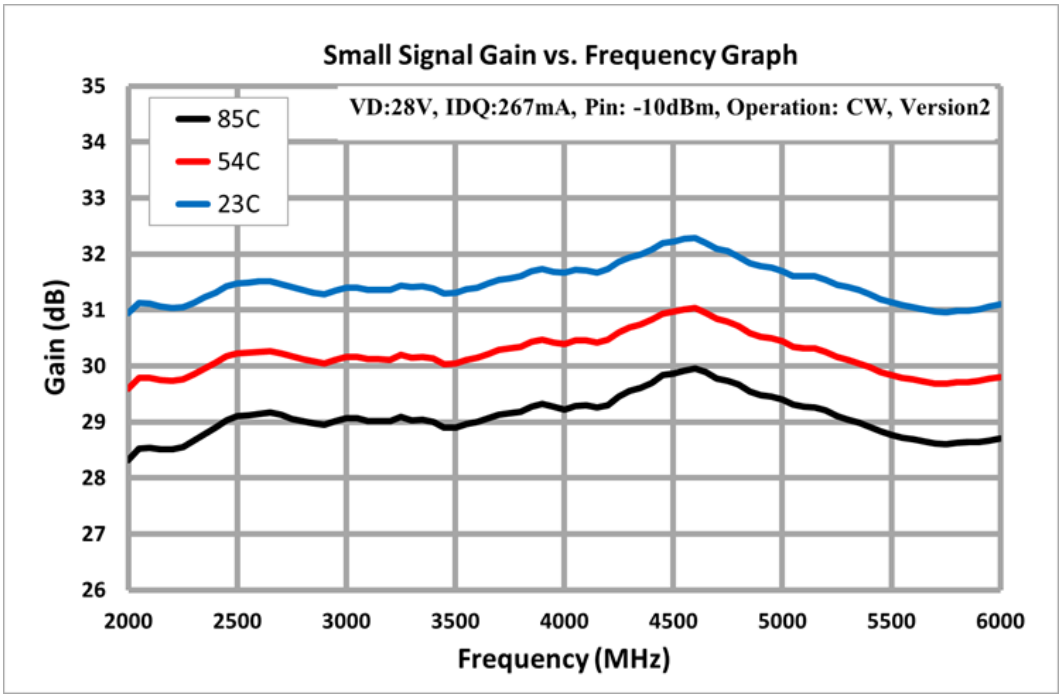


Figure 4.25. Small Signal Gain vs. Frequency Graph vs. Temperature

All these on-wafer and connectorized module measurements show that 5 W output power and 40% PAE targets are achieved at room temperature for version-2. Output power is equal or higher than 38 dBm for 2-6 GHz even at 85ºC. Small signal gain is around 29 dB at 85ºC. Large signal gain is larger than 22 dB at saturation and flatness is around ±0.4 dB which is well for this broadband amplifier. Tuning harmonic impedances in output matching increases the RF performance as expected. Another important point of this thesis work is the first run success. For small signal characteristics, transistor S-Parameter measurements are used and for large signal characteristics, PDK models are used.

CHAPTER 5

CONCLUSION AND FUTURE WORK

In this thesis, two stage 2-6 GHz 5 W MMIC amplifier is designed with commercially avaliable 0.25 μm GaN on SiC process including simulation, fabrication and measurement processes. The design is started with technology, transistor size and topology selection. To satisfy high gain and high power requirements at lower area, GaN on SiC process is chosen. Transistor sizes are arranged with respect to power, efficiency and gain requirements by considering process output power density and matching losses. A 8x200 μm transistor is chosen for the power stage while a 6x90 μm transistor is used for driver stage of the die. Reactive matching topology is chosen because of it's high gain and high output power properties. The challenging part of this topology is the broadband operation frequency which requires flat responses during all band. The die design is continued with load-pull and S-Parameter measurements of transistors. Both these transistor's measurements and PDK transistor large signal models are used to achieve first-run success. One of the versions is designed by S-Parameter measurements to simulate small signal responses correctly and other version is designed by PDK transistor large signal models by considering harmonic impedances in output matching. Designing two versions increases the chance of first-run success. Stability analysis, matching designs of stages and EM simulations are finalized before fabrication. First version is fabricated in $3 \times 3\ mm^2$ area while second version area is $2.89 \times 3\ mm^2$.

Both small signal and large signal measurements are performed by on-wafer and connectorized module measurement setups. It is observed that measurements are consistent with simulations for both small signal and large signal characteristics. Version-2 has better large signal responses as expected, so it's chosen as major version to analyze in detail. Between 28.3 dB minimum and 30 dB maximum, average 29 dB, small signal gain is obtained at 85°C temperature which is quite high.

Gain flatness is around 0.85 dB and this level is acceptable for a reactive matching amplifier at this broadband operation. The MMIC has larger than 15 dB input return loss and 6 dB output return loss. Average 38.4 dBm output power with minimum 37.6 dBm is obtained at saturation. This means that larger than 5 W output power is achieved. Minimum obtained PAE is 36% and maximum PAE is 46% in 2-6 GHz operation frequencies. Average 22.5 dB large signal gain is measured at saturation, 7 dB gain compression. RF performances of the die is summarized in Table 5.1.

This work has 6.3 W / 8.67 mm^2 ≅ 0.72 W/mm^2 power density which is larger than TGA2597 which is also 0.25 μm GaN process die [22]. Only one version-2 die can used to achieve same power and gain rather than 2 or 3 TGA2597. This improves the whole RF system about price and dimension, because dividers, combiners and other RF components should be used in case of TGA2597. The performance of the work is compared with another GaN die examples as well [26, 27]. This RF performances comparison of dies are shown in Table 5.2. This work has higher gain and higher output power performances with more power density with respect to other works.

Table 5.1. RF Performances of the die

Parameter	Units	Minimum	Typical	Maximum
Frequency Range	GHz	2		6
Input Return Loss (S11)	dB	15	16	19.5
Output Return Loss (S11)	dB	6	9	15
Small Signal Gain (S21)	dB	28.3	29	30
Large Signal Gain	dB		22.5	
Output Power	dBm	37.6	38.4	39
PAE	%	36	38	46

Table 5.2. RF Performances Comparison

	Process	BW [GHz]	Gain [dB]	Pout [W]	PAE [%]	Size [mm²]	Power Density [W/mm²]
This Work	**GaN**	**2-6.2**	**29**	**6.3**	**36**	**8.67**	**0.72**
Qorvo [22]	GaN	2-6	21	1.6	31	3.21	0.47
Sainty-Tech [26]	GaN	2-6.5	25	2	38	3.01	0.66
Reference [27]	GaN	2-6	18	7	25	23.04	0.30

Packaging of the MMIC can be concidered as a future work. The die can be used as MMIC directly, but it's better to have a package option for RF systems. This makes easier and safer to use in a RF module. Proper package structure should be investigated for this $2.89 \times 3\ mm^2$ GaN on SiC die. Air cavity quad-flat no-leads (QFN) package is an example for this packaging work. Simulations would be performed to observe wire-bond effects on the selected package. Another future work can be a high power amplifier, such as 2-6 GHz 30 W power amplifier. Since simulations and measurements are coincidence, higher performance design can be performed as well. Also, same transistor measurements and PDK models can be used for this high power amplifier.

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